HOME COMPUTER
NEW TECHNICIAN GUIDE

TEXAS INSTRUMENTS HOME COMPUTER NEW TECHNICIAN GUIDE

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TI 99/4 HOME COMPUTER

THE TI 99/4 HOME COMPUTER

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INTRODUCTION:

The TI 99/4 Home Computer was initially presented at the Consumer Electronics Show in June 1979 by Texas Instruments. The TI 99/4 is a TMS 9900-based microprocessor system. Presently, the 99/4 mainframe, along with available peripherals, are being manufactured by the Consumer Products Division of Texas Instruments, Inc. in Lubbock, Texas.

The TI 99/4 has many key features. Some of these feature include 16-color graphics, music and sound over four octaves, plus a built-in equation calculator. The TI 99/4 also makes use of an expanded TI Basic. This feature plus the capability for up to 72K bytes of memory (16K RAM internal, 26K ROM, and up to 30K ROM interfaced via the Command Module peripherals) make the TI 99/4 Home Computer a very powerful tool. These key features and the general operation of the TI 99/4 will be presented in the following pages.

SYSTEM BLOCK DIAGRAM:

The TI 99/4 Home Computer effectively combines each of the individual features of the unit into a complete and complex system. The basic blocks of the system include the CPU, sound generation, video display, I/O control, plus timing and control logic. These features are interfaced to produce the complete microprocessor system. The system block diagram of the TI 99/4 is shown on Figure 1. As can be determined from the diagram, the additional circuitry for 16-to-8 bit data

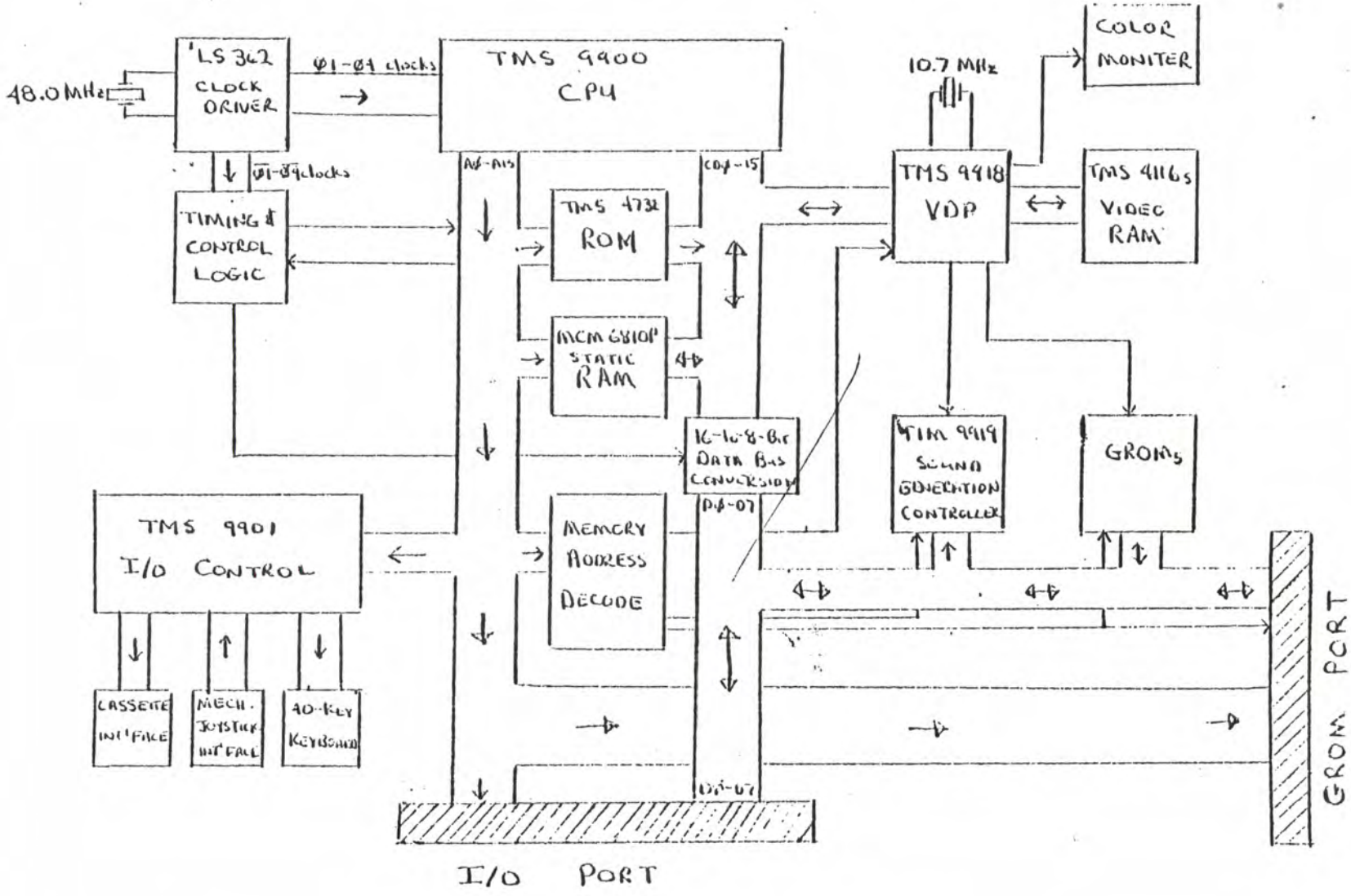


Figure 1. TI 99/4 Home Computer System Block Diagram

bus conversion and memory address decode are also used in the operation of the system.

CPU:

The heart of the TI 99/4 Home Computer is the TMS 9900 microprocessor, a 16-bit CPU. The TMS version of the 9900 is manufactured using N-channel, isoplanar, MOS technology (NMOS). Some of the key features and characteristics of this CPU include the following:

* Separate data and address busses
* Multiple register file capability
* Sixteen bit data word size
* Fifteen bit address word size
* Sixteen to forty-eight bit instruction word size
* Sixty-nine basic instructions
* Three dedicated I/O control lines
* 2 usec instruction cycle time
* 3.0 MHz max clock frequency
* Four phase clock / 12v voltage swing
* Three supply voltage levels required
  +5v / 75 mA
  -5v / 0.1 mA
  +12 / 40 mA
* Sixty-four pin DIP package

As just stated the TMS 9900 is a 64-pin DIP. Of these 64 pins, fifteen comprise the tri-state address bus. This bus contains the address of a desired memory location in an

external memory device. The data bus takes up sixteen pins on the TMS 9900. This tri-state, bidirectional bus carries information to and from the 9900, from external memory and I/O devices. An additional six pins are reserved for the supply voltages, one each for the -5v and +12v supplies and two each for +5v supply and ground reference. Four pins of the 9900 are used for the four phase clocks required by the system. The remaining eighteen pins are used for control signals. These signals and a brief description of their functions follow:

* WAIT - An output signal which when active indicates that the 9900 is waiting for the external memory system to enter a ready-condition before continuing its operation.
* $\overline{\text{LOAD}}$ - With this signal active, the 9900 executes a non-maskable interrupt with a specific memory address.
* $\overline{\text{HOLDA}}$ - An output signal which indicates that the 9900 is in a hold state awaiting the completion of a memory cycle.
* $\overline{\text{RESET}}$ - When active, resets the 9900. When initially deactivated, the CPU starts an interrupt sequence, clears the status register, and begins execution.
* IAQ - An output signal which when active indicates that the 9900 is acquiring an instruction.
* DBIN - An output signal which when active allows data to be placed on the data bus by the external memory system.

* CRUOUT - When an LDCR, SBO, or SBZ instruction is being executed, serial I/O data will appear on the CRUPUT line.
* CRUIN - Receives data from external interface logic.
* $\overline{\text{INTREQ}}$ - An input signal which when active indicates an external interrupt is requested.
* IC3(LSB), IC2, IC1, IC0(MSB) - The four input signals which comprise the interrupt code and indicate the priority level of the interrupt.
* CRUCLK - An output signal indicating that the sampling of the CRUOUT data or decoding of A1-A2 should be done by the external interface logic.
* $\overline{\text{WE}}$ - An output signal indicating that the 9900 has data to be written into the external memory system.
* READY - An input signal which when active indicates that the external memory system is ready to read or write in the next clock cycle.
* $\overline{\text{MEMEN}}$ - An output signal which when active indicates that the address bus contains an address in memory.
* $\overline{\text{HOLD}}$ - An input signal which when active indicates to the CPU that an external controller wants to use the address and data bus to transfer information to and from the external memory system.

A study of the TMS 9900's internal structure is a useful tool when trying to understand the operation of the IC. The architecture of the 9900 microprocessor is shown in the diagram of Figure 2. This shows the internal features within

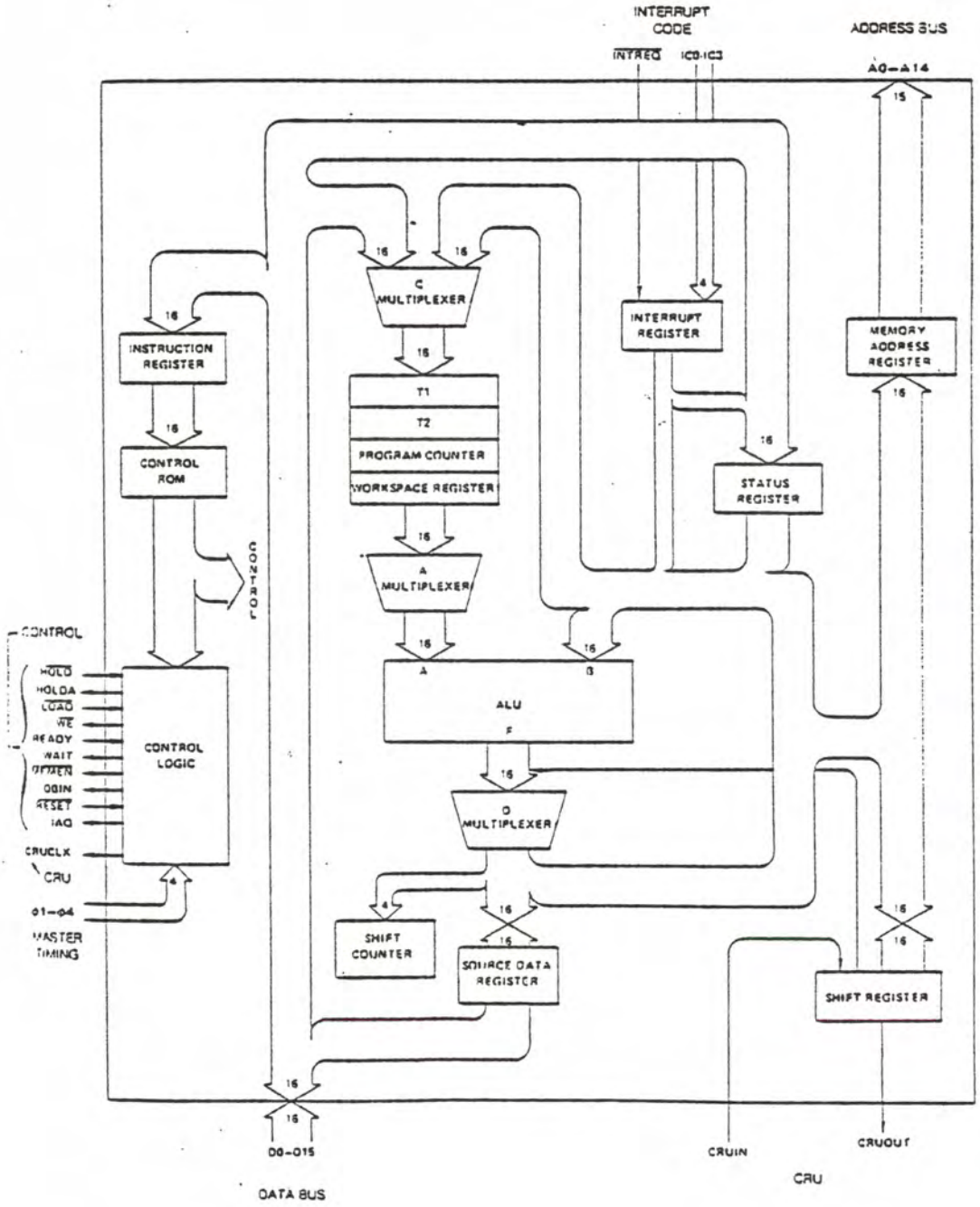


Figure 2. TMS 9900 ARCHITECTURE

the CPU. These features include:

* The ALU
* 3 multiplexer busses
* Control logic and control ROM
* Internal registers

  Memory address register, shift register, status register, interrupt register, source data register, shift counter, workspace register, instruction register, and auxillary registers T1 and T2.

The ALU (Arithmetic Logic Unit) is a 16-bit, parallel logic network used in the execution of the 9900's instructions. This unit performs arithmetic functions, logic, and comparisons. The multiplexer busses are used in the transfer or flow of data in the CPU. The control circuitry provides the signals necessary for correct gating.

The control logic and control ROM provide the necessary signals for the correct sequencing or operation of the CPU's instructions. This is accomplished with the aid of the input control signals and the master timing. Among the internal register there are three which are "the key architectural features" of the CPU. These registers are the workspace pointers, the program counter, and the status register. The workspace pointer contains the location of the first word in the workspace. The program counter contains the address for the next word which is to be used in the execution of an instruction. The status register determines if the conditions necessary for an instruction execution have been met. This is

done by the setting of flags.

In the operation of the 9900, sixty-nine instruction words can be used. A list of the 9900's instruction set can be found in Table 1. These instructions are used to perform arithmetic operations, logic, comparisons, and manipulation operations on data. They are also used for the loading and storing of data within the CPU's internal registers. Data transfer between the external memory system and external devices is also made possible with the instructions via the CRU. Instructions are also used as control functions with the CPU.

The external memory system used with the TMS 9900 in the TI 99/4 consists of 2-TMS 4732's and 2-MCM 6810P's. The TMS 4732s are 4K x 8 bit ROMs and are addressed via lines A3-A14 of the address bus. However, one of the 4732s uses the DØ-D7 lines on the data bus while the other uses data lines D8-D15, thus combining the 2-4732s into a 4K x 16 bit ROM. The MCM 6810Ps are 128 x 8 bit static RAMS and are used as a scratch-pad by the CPU. In a manner similar to the 4732s, the two 6810s are combined to form a 128 x 16 bit RAM. One slight difference from the 4732s is that the 6810s are addressed by address lines A8-A14.

The 9900 uses three control signals during operation of the external memory read and write to control the use of the address and data busses. These signals are DBIN, $\overline{\text{MEMEN}}$, and $\overline{\text{WE}}$. During memory read, DBIN and $\overline{\text{MEMEN}}$ are active, while $\overline{\text{WE}}$ is not. The active signals allow an output onto the address bus indicating the desired memory location to be read.

The DBIN and $\overline{\text{MEMEN}}$ also deactivate the data bus output. Drivers are deactivated to prevent the input data from conflicting with output data. Memory write makes use of $\overline{\text{MEMEN}}$ and $\overline{\text{WE}}$ both active, and DBIN deactivated. Under these conditions the 9900 outputs on the address and data busses and holds these outputs for the time required by the RAM.

An additional circuit in the TI 99/4 Home Computer works in the 9900 and memory devices. This is the 16-to-8 bit data bus conversion. The TI 99/4 is an 8-bit I/O data system. Because of this, all the circuits outside the 9900 operate on 8-bit data words. Since the TMS 9900 operates with a 16-bit data bus, the 16-to-8 bit data bus convertor is an obvious need.

The 16-to-8 bit data bus conversion circuit makes use of bus tranceivers (74LS245), D-latches (74LS373), and buffers/line drivers (74LS244) as shown in Figure 3. The DBIN signal from the 9900 and the QC signal from the timing and control logic circuit are the control signals in this circuit. In the 16-to-8 bit conversion, DBIN is used to determine when the DØ-D7 data from the 9900 and memory are sent to the system data bus through the tranceivers and when the D8-D15 data is sent through the line drivers. Thus, one 16-bit data word is converted to two 8-bit data words. The QC signal aids in the control of the 8-to-16 bit data bus conversion. During this conversion, the QC signal allows the first data word through the transceivers to the 9900's DØ-D7 data lines. The purpose of the D-latches is to bypass the line drivers (74LS244) to get to the 9900 data bus. The se-

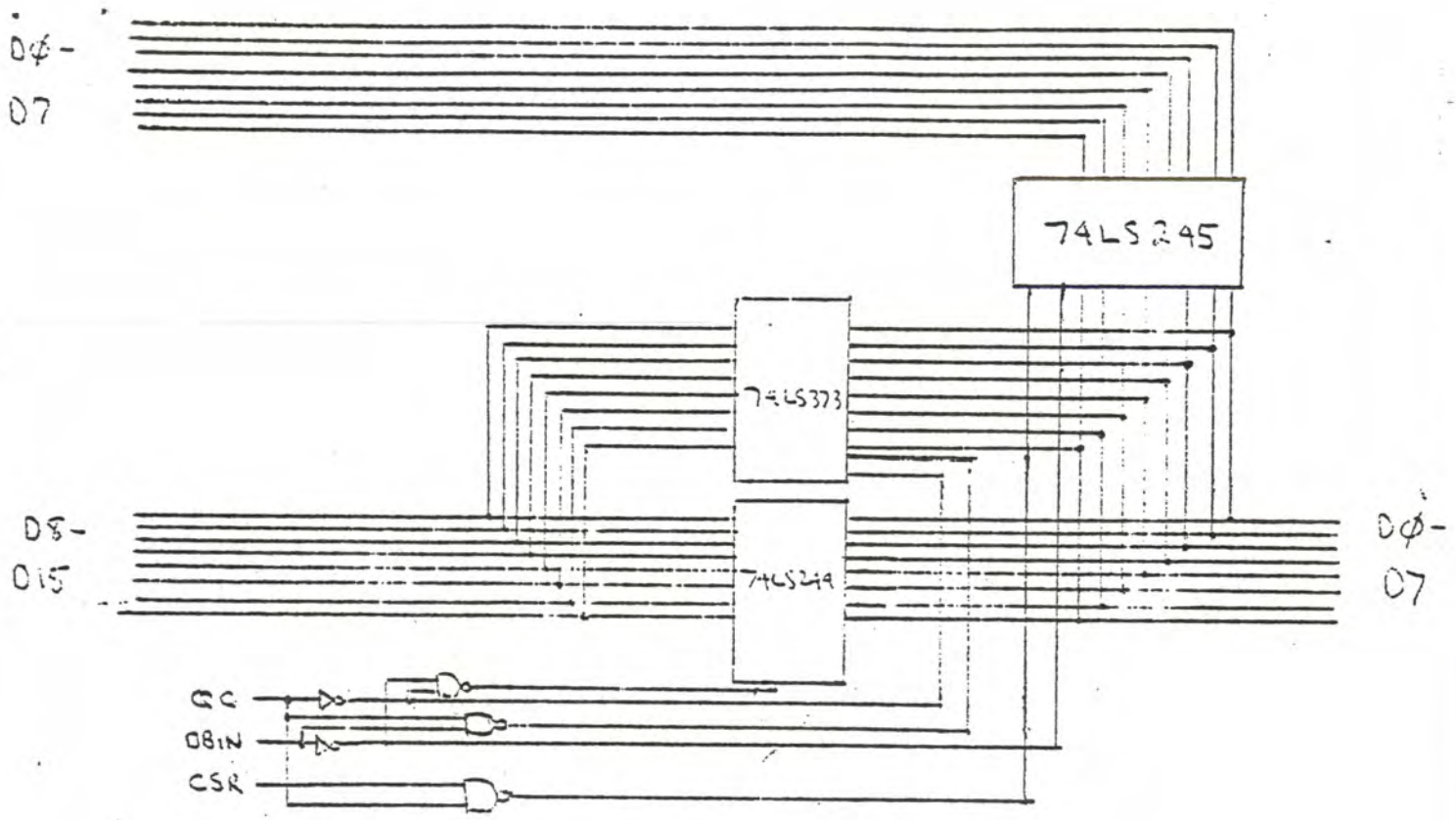


Figure 3. 16-to-8 Bit Data Bus Conversion

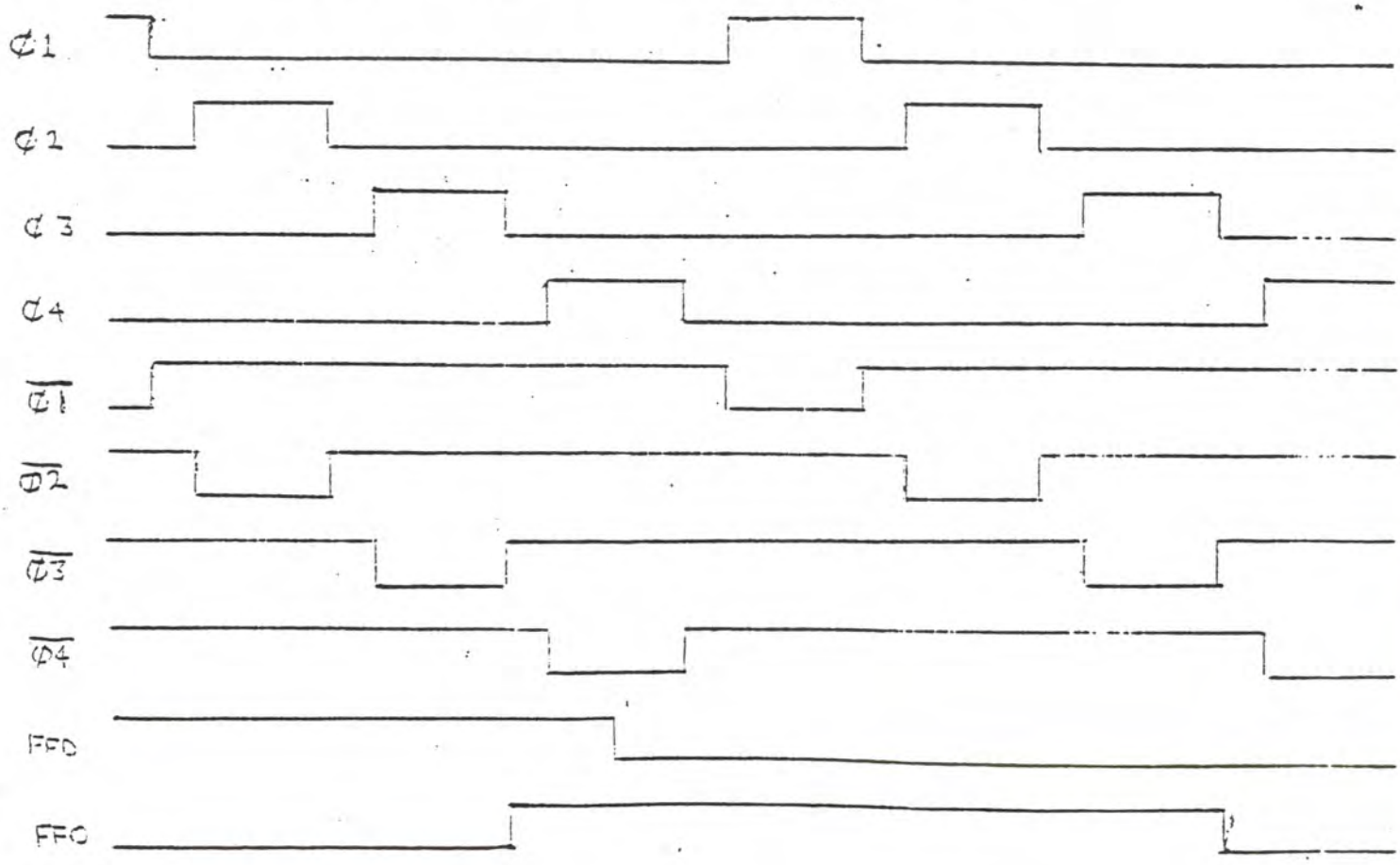


Figure 4

cond data word is latched-on by the D-latches and driven to the 9900 D8-D15 data lines around the line drivers. Thus, the two 8-bit data words used by the system are converted to a 16-bit data word used by the 9900.

Another circuit used closely with the 9900 and external memory system is the memory address decode circuit. The memory address decode takes the CPU control signals and outputs supplementary signals which insure the proper operation of all memory devices within the TI 99/4 Home Computer.

The memory address decode circuit consists of two 3-to-8 line decoders (74Ls138) and 2-input Nand gates (74LS03). The first decoder works by taking the AØ-A2 address lines and MEMEN and sending the ROMEN, MBE, ROMG, and MB4 signals to operate in the system ROM and in the control logic. The second decoder takes A5B-A3B signals from the Internal GROMS along with DBIN to send Sound SEL, VDP R, VDP W, SBE, and READY/$\overline{\text{HOLD}}$ signals to the GROMS, VDP, sound chip and control logic.

TIMING AND CONTROL LOGIC:

As previously mentioned, the TMS 9900 requires a 4-phase clock. As such, the timing and synchronization within the TI 99/4 system must be critically precise. The key to this timing is the 74LS362, a 4-phase clock generator/driver made especially for use with the TMS 9900. Some of the key features of the 74LS362 include the following:

* 4 phase Hi-level (+12v) clocks

* 4 phase Low-level (+5v) clocks
* Internal oscillator (controlled by crystal or capacitor) or External oscillator can be used
* Clocked D Flip Flop used for system reset signal synchronization
* Power requirements: +5v, +12v
* Packaged as 20 pin DIP

The 'LS362 as used in the TI 99/4 uses a quartz crystal to provide a 48.0 MHz reference frequency. An LC tank circuit selects the desired crystal overtone, in this case the third overtone, and establishes the internal oscillator frequency. The frequency of oscillation can be determined from the formula

$$f_{osc} = \frac{1}{2\pi\sqrt{LC}} . \qquad (1)$$

The clock frequencies in the TI 99/4 system, operate at the TMS 9900 max frequency of 3.0 MHz.

The 'LS362 requires two supply voltages +5 volts and + 12 volts. These supply voltages provide for the eight clock outputs of the 'LS362. The outputs include the 4-phase Hi level (+12v) clocks required by the TMS 9900 and the 4-phase low level (+5v) complementary clocks. The latter clocks are TTL compatible and are used in the timing of the state logic. One additional output comes from the internal D-type flip flop. The data (D) signal comes from the +5v supply when power is applied to the TI 99/4 system. The flip flop output is used as the RESET into the 9900. This serves to synchronize the 'LS362 clocks and TMS 9900. The clock outputs

and the flip flop I/O are shown on Figure 4.

The +5v complementary clocks are helpful in understanding the control logic portion of the TI 99/4. The control logic consists of D-type flip-flops (74LS74), a 4-bit bidirectional shift register (74LS194), plus assorted gates. The gates include inverters (74LS04), 2-input NAND gates (74LS00), and 2-input OR gates (74LS32). Since the control logic is timed by the complementary clocks, the effect of each clock into the logic can be discussed.

The first low-level clock phase $\overline{\text{Ø1}}$ is used to clock the 74LS194 shift register. The shift register is used to synchronize the $\overline{\text{MEMEN}}$ signal from the 9900 plus the A3-A5 address bus lines with the SYNCHO READY, ROMEN, and MB4 signals from the memory address decode circuit. The shift register in turn provides the primary READY signal for the 9900 (QA), a preset signal for the D Flip-Flop B (QB), and the QC signal. The QC signal is used directly as an enable signal into the memory address decode circuit, as a GROM PORT I/O signal, and as a control signal into the 16-to-8 bit data bus conversion circuit.

The phase 2 clock (Ø2) is used to clock D Flip-Flop A. This flip-flop takes the system ready signal, also from the memory address decode, to 'sync' to SNYCHD READY to the 9900 READY signal and 74LS194 shift register.

The phase 3 clock (Ø3) is not used in this portion of the control logic, but is used in timing the TMS 9901 and is also the I/O clock.

The final clock used in the control logic portion is the phase 4 clock (Ø4). It is used to clock D Flip-Flop B. This flip-flop uses the memory address decode signals and the $\overline{\text{ME}}$-$\overline{\text{MEN}}$ signal, via the QB and QC outputs from the shift register, to control the WE signal in the memory address decode circuit, to the sound generator I.C., and to the I/O port.

I/O CONTROL:

The I/O Control circuit consists of the Programmable Systems Interface (PSI TMS 9901), the Mechanical Joystick circuit, the Keyboard, and Cassette Interface. However, the key element in this circuit is the TMS 9901. The TMS 9901 is manufactured using N-channel, silicon-gate MOS technology (NMOS). Some of the key features of this component include:

* Single phase clock ($\overline{Ø3}$ from 74LS362)
* 9900-Family Peripheral (easily interfaced to TMS 9900)
* I/O Interface and Interrupt Capability
* TTL Compatible I/O
* Single +5 volts Supply voltage
* Packaged as a 40-pin DIP

The TMS 9901 consists of three groups of internal buffers, CRU logic, an Internal Timer, and a Prioritizer and encoder, as seen in Figure 5. The internal buffers are used with the I/O Interface and Interrupt lines. These buffers are MOS to TTL buffers and have a fan-out capability of two. The first group of buffers work with the six dedicated Interrupt lines, while the second group of buffers work with the

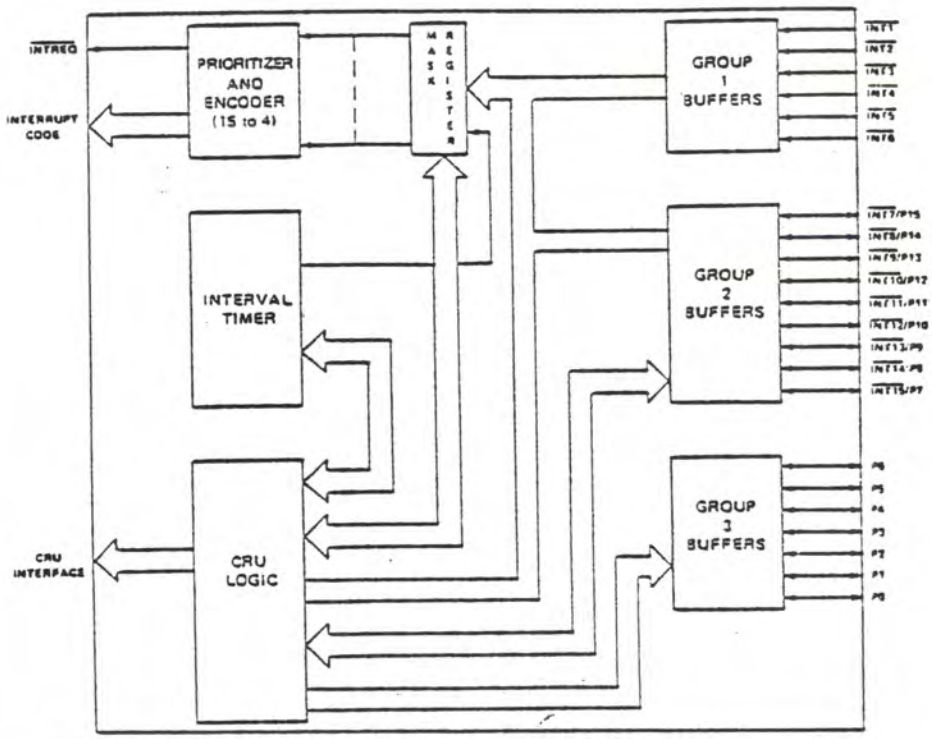


Figure 5. TMS 9901 Architecture

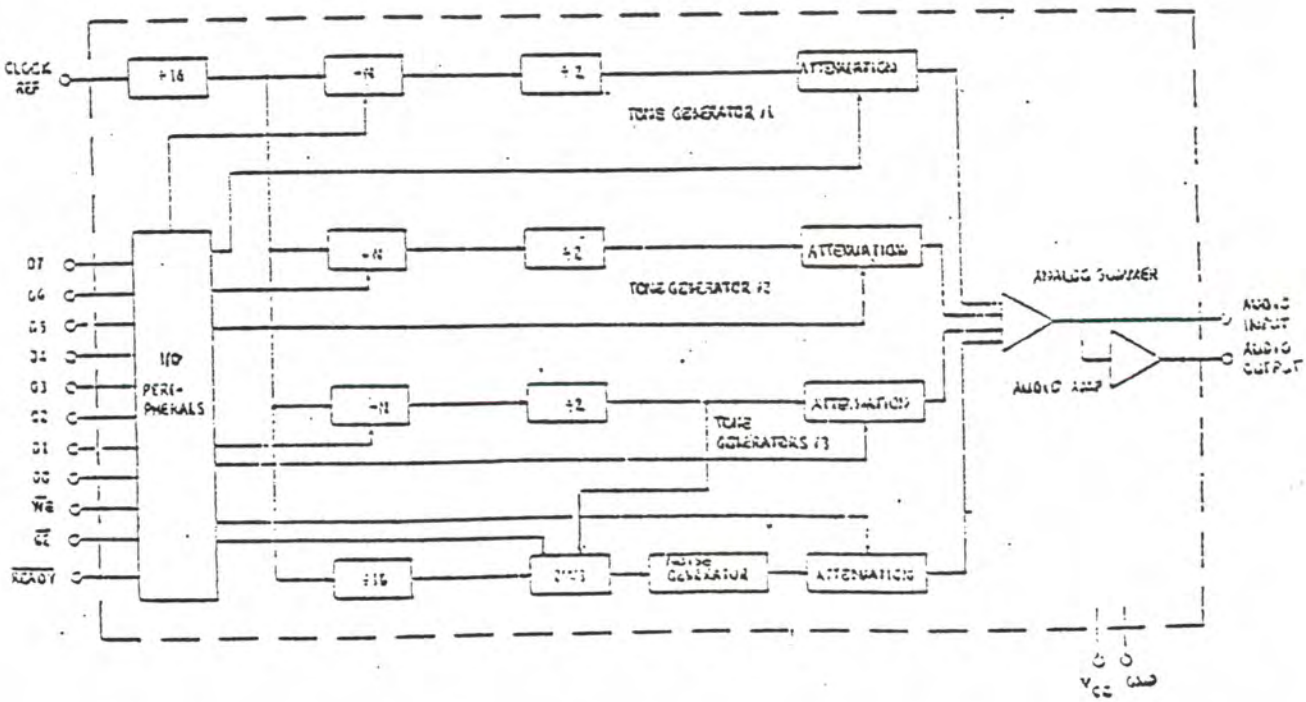


Figure 6. TIM 9919 Architecture

nine programmable lines which can be used as either I/O or Interrupt lines. The final group of buffers work with the seven dedicated lines(I/O).

The fifteen available Interrupt lines, six dedicated and nine programmable are used to send a 15-bit signal through the Mask Register to the Prioritizer and Encoder section and also to CRU logic. In the Prioritizer and Encoder section, the 15-bit signal is assigned an interrupt priority and converted to a 4-bit Interrupt code. This section also provides the Interrupt REQUEST (INTREQ) signal for the CPU.

The sixteen available I/O lines, seven dedicated and nine programmable, are transferred directly from the CRU logic, through the buffers, and to the I/O pins. Also available are any unused dedicated Interrupt lines as input data lines. Actually there is a possibility of up to 22 input lines.

The CRU logic is the control center of the component. The TMS 9900 control signals and $\overline{\text{Ø3}}$ clock used for timing are linked to the 9901 via the CRU Interface. The control signals from the CPU are CRUIN, CRUOUT, CRUCLK, $\overline{\text{RSTI}}$, $\overline{\text{CE}}$, and 5 address select lines. CRUIN, an output signal from the 9901, is used to send data specified by the address select lines. CRUOUT is sampled by the 9901 when CRUCLK is active. The data sampled is written into a specified command bit. The 9900 alerts the 9901 that data is available on the CRUOUT line by activating CRUCLK. The signals $\overline{\text{CE}}$ and $\overline{\text{RST1}}$ do not come directly from the 9900 but go through special logic entering the CRU Interface. Power Up Reset, $\overline{\text{RSTI}}$, when active resets the

mask register, clears the Interrupt code, and programs the I/O lines to inputs.

Chip Enable, $\overline{CE}$, is used to allow data through the CRU Interface to the CPU. The address select lines are used to indicate the data bit accessed by the CRU Interface. In the 9901, the Interval Timer is used in the Interrupt control. Interrupts are caused whenever the clock is enabled. Disabling the Interval clock prevents the component from interrupting.

The Interval Timer is also used with the cassette interface. This interface is software intensive and depends on the Interval Timer for timing. The cassette interface operates with BYTE/Manchester Encoding format. Some key points of this interface include:

* I/O Wave Shaping to increase reliability
* Two Motor Control Circuits
* Has Capability for Cassette Read/Write

The cassette interface requires the use of five I/O lines from the 9901; of these, four are programmable. Four lines are used as output lines, two for the cassette motor controls 1 and 2, and two for the cassette MAG OUT. The input line is used for the MAG IN signal. The Audio-In signal to the TIM 9919 is also generated in the cassette circuit to enable the user to hear the cassette I/O data either on a moniter or an audio board.

The cassette motor control circuit makes use of four TIS 92 transistors and two TIL 119, opto-isolator transistors. This circuit provides an enable/disable signal to the cassette

motor control on the cassette peripheral. The MAG OUT circuit takes the output from a programmable I/O line on the 9901 across a resistor-capacitor filtering circuit directly to the MAG OUT line. The MAG IN line uses two 4558 operational amplifiers. The first op-amp is used as an amplifier with a negative feedback network while the second takes the first's signal and modifies it into a usable TTL compatible input signal to the 9901.

The Mechanical Joystick Interface and the 40-key keyboard both make use of a 2-line-to-4-line decoder/demultiplexer (74LS156) in their interface with the TMS 9901. The joystick interface utilizes 5 Interrupt lines, 4 dedicated and 1 programmable, and two dedicated I/O lines. The Interrupt lines receive data from the joysticks by means of loading down the normally high lines. The two I/O lines are used to send data to the 2-line-to-4-line demultiplexer by enabling the joysticks. By enabling the joysticks, data is inputted through the interface to the 9901.

The 40-key keyboard uses three dedicated I/O lines and eight Interrupt lines, 4 dedicated and 4 programmable. The keyboard is divided into two 20-key sections, each 4 rows by 5 columns. The row data is sent directly to the Interrupt lines while the column data goes through the demultiplexers to the I/O lines. All of the keyboard lines are normally high.

SOUND GENERATION:

Another of the TI 99/4's key features is sound generation.

The key to music and sound generation within the system is TIM 9919 (SN 76489) Sound Generation Controller. The 9919 provides sound in three tones and over four octaves. Some of the features within the sound chip are listed:

* Three Programmable Tone Generators
* Programmable White Noise Generator
* Programmable Attenuation
* TTL Compatible
* 3.579 MHz Reference Clock
* Allows Simultaneous Sounds
* 8-ohm Speaker Drive Capability
* Single +5 volt Power Supply
* Packaged as 16-pin DIP

The TIM 9919 is a TTL compatible I^2L/Bipolar IC. Designed especially for use in microprocessor systems, it comes in a 16-pin DIP. The sound chip has 8 pins for input data bus lines. It also has 2 pins for its power requirements, one for +5v supply and one for ground reference. The remaining five signals are used for control and timing signals plus audio I/O. The TIM 9919 requires a 3.59MHz clock for a reference frequency in its sound generation. The 9900 also supplies three control signals ($\overline{CE}$, READY, and DBIN) to the sound chip. The remaining two pins are used for Audio Signal In and Audio Drive Out.

The TIM 9919 is made up of three programmable tone generators, a programmable noise generator, a clock scalor, individual generator attenuators and an audio summer output buffer. The TIM 9919's architecture can be seen in Figure 6. The three

programmable tone generators are composed of a frequency synthesis section and an attenuation section. The tone generators require two data words to operate. The frequency synthesis section uses a 10-bit input data word to produce an output signal of the desired frequency. This desired frequency is then inputted into a four-stage attenuator along with the four remaining input data bits to provide a maximum attenuation of 28 dB.

The noise generator is also composed of two sections, a noise source and an attenuator. The noise source is made of a shift register utilizing an exclusive OR feedback system and resulting in either Periodic or White noise generation. This output is also inputted to an attenuator to provide a maximum of 28 dB attenuation.

The audio summer/output buffer is an operational amplifier summing circuit. This circuit sums up the three tone generator outputs, the noise generator output, and the Audio Signal In. This allows for simultaneous sound. The output buffer can then send this signal out at up to 100 mA into an 8-ohm speaker load.

The sound chip receives three control signals from the CPU. These are the $\overline{CE}$ (Chip Select), $\overline{WE}$ (Write Enable), and READY signals. The $\overline{WE}$ signal when active indicates that the data bus has information from the 9900 available. The READY signal is activated when the sound chip has completed reading the data. $\overline{CE}$ is activated when data is able to be transferred from the 9900 to the sound chip.

The data bus into the TIM 9919 is also taken in parallel to the GROMs. The GROMs are 0430 Graphics ROM each 6K x 8 bits. The three GROMs in the TI 99/4 Home Computer system contains all the information on the TI Basic usage and the Basic routines. The internal GROMs can be expanded by means of external GROMs on Command Module Peripherals. Accessing the internal GROMs is through the GROM Port on the mainframe top side.

There are five control signals into the GROMs. These are DBIN, GR, GRC, GS, and A14. DBIN, as previously explained, indicated when the data bus can be accessed. GROM READY (GR), when active, indicates that the GROM is ready to send data over the data bus. GROM READY CLK (GRC) is the GROM timing clock which synchronizes the VDP with the GROMs. GROM Select (GS) is a GROM input signal from the 9900 logic indicating that the system is prepared to receive the GROMs' data. The GROMs require two power supplies, a +5volt supply and -5volt supply.

VIDEO DISPLAY:

Video Display is another one of the key features in the TI 99/4 Home Computer. This portion of the system is composed of the TMS 9918 Video Display Processor (VDP), eight TMS 4116 (16K x 1) dynamic RAMs, an external crystal circuit, and an external video drive circuit. Of these parts, the most vital to the operation of this circuit is the VDP. Some of the key features of the TMS 9918 include:

* Three video color display modes
* 9900 interface requires a minimum of additional circuitry
* Can address 4-16K bytes of RAM for CPU or display
* Provides eight colors with two luminous levels each
* 10.74 MHz internal crystal oscillator
* Provides GROMCLK and CPU Clock to TI 99/4 system
* Requires single +5 volt power supply
* Packaged as 40-pin DIP
* Manufactured using N-channel MOS technology (NMOS)

The VDP is a very independent IC, requiring only the CPU control lines to operate within the TI 99/4. This is supported by the fact that the VDP supplies all the video, control, and synchronization signals needed. Also, the VDP controls the transfer of display data and the data refresh required by the TMS 4116 dynamic RAMs. The VDP signals are interfaced into the system as to require little additional circuitry.

Another key feature of the VDP is the three video color display modes. The VDP has pattern graphics, multicolor, and text display modes. The pattern graphics are used mainly with the game and educational aspects of the TI 99/4. It provides a 256 x 192 pixel display in 16 possible colors. The multicolor mode provides a 68 x 48 dot display which is also available in 16 colors. The text mode is used mostly with computer type displays. It uses 24 lines of 40 characters but is used with only two possible colors.

The complexity of the VDP's internal structure can be seen in its block diagram shown in Figure 7. The multiple

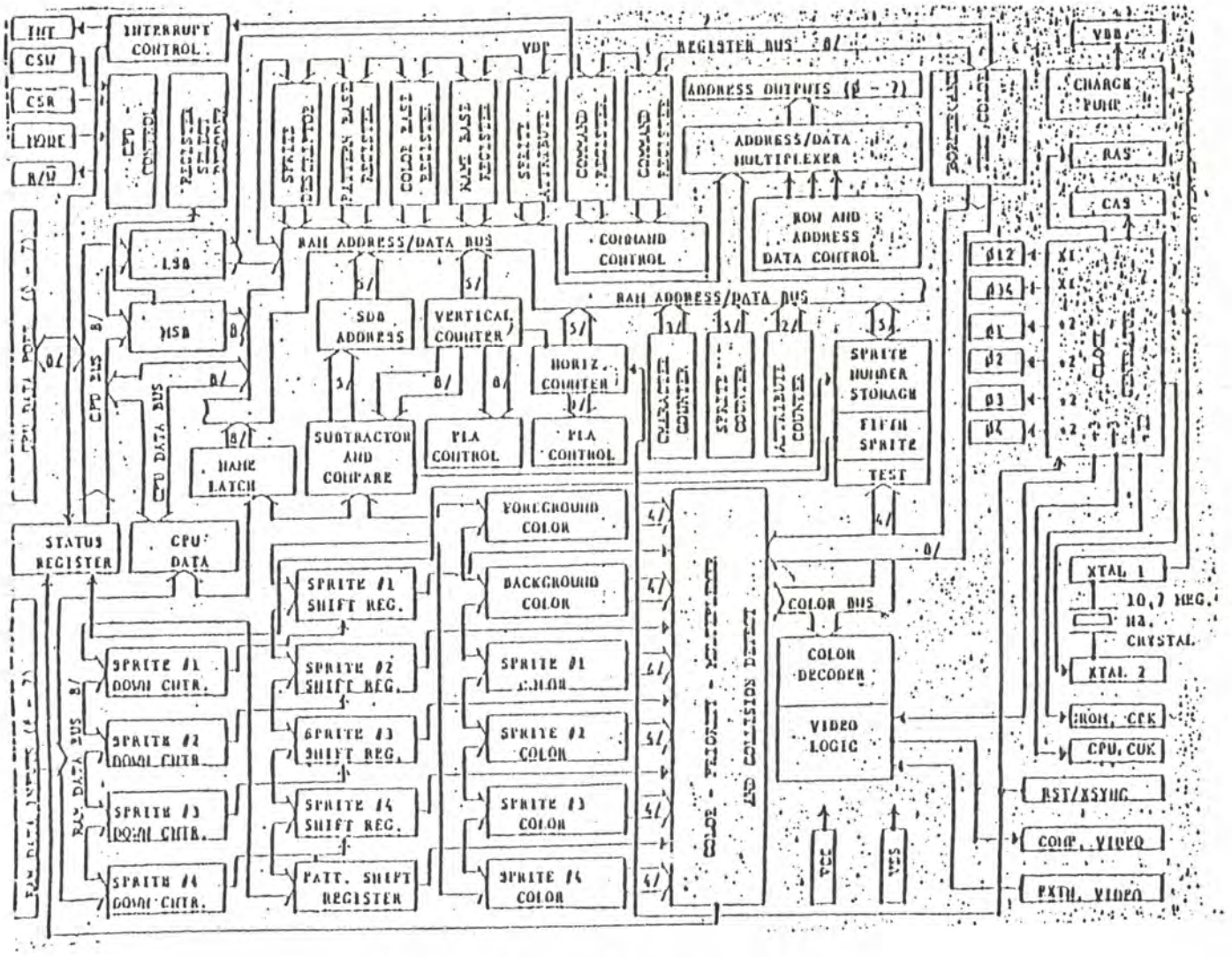


Figure 7. TMS 9918 Architecture

counters, registers, and internal control logic require a detailed study to properly understand the entire functions within the VDP. However fairly evident are the IC's I/O. These include the data busses, address busses, and control lines.

The first data bus, the CPU Data Bus, is used to interface the VDP with the 9900. This eight-bit bidirectional bus is controlled by two select lines plus an address line. The other data bus, also 8-bits, is used with the 8-bit RAM Address/Data Bus, and three control lines to interface the 4116 dynamic RAMs with the VDP. The VDP output control signals and a brief description of each include:

* CAS - The 4116 RAM column address strobe
* RAS - The 4116 RAM row address strobe
* R/N - Dynamic RAM WRITE signal
* INT - CPU Interrupt from the VDP
* COMVID - NTSC composite video output
* GROMCLK - VDP output clock used synchronizing the VDP with and providing the timing for the GROMs.
* CPUCLK - NTSC color burst frequency clock

The control lines into the 9918 and a brief discription of each include:

* MODE - CPU interface mode select
* CSR - CPU-VDP read strobe
* CSW - CPU-VDP write strobe
* EXTVID - External video input
* $XTAL_1$, $XTAL_2$ - Inputs from the external crystal oscillator

The VDP uses a crystal oscillator circuit in its operation. This circuit uses a fundamental frequency crystal to provide the VDP with a reference frequency for the internal oscillator. The internal oscillator is the main timer for all the internal VDP clocks and for the output clocks. The master clock (internal oscillator) provides an internal pixel clock at a 5.3 MHz frequency by dividing the reference frequency (10.738635 MHz) by a factor of two. In a similar manner, the CPU clock a 3.58 MHz frequency signal is the reference frequency divided by three. The reference frequency divided by 24 provides the GROMCLK signal.

The VDP also makes use of the Video RAM circuitry. The Video RAMs, 4116's, are interfaced to the VDP by an 8-bit data bus, an 8-bit bidirectional RAM address/data bus, plus three control signals $\overline{RAS}$, $\overline{CAS}$, and R/$\overline{W}$. This VDP- RAM interfacing is shown in block diagram form in Figure 8. This interfacing requires very little additional electronic circuitry. The eight TMS 4116's are 16K x 1 bit dynamic RAMs and are interfaced in such a fashion as to provide a 16K x 8 bit Video RAM. The 4116s require the three supply voltages available in the 99/4 system, -5v,+5v, and +12v.

The VDP puts out a composite video signal which goes through a transistor-resistor network to provide a compatible video output to the TI 99/4 Color Moniter. The 99/4 can be interfaced to a regular television by modulating a composite video signal to television frequencies by an external RF modulator.

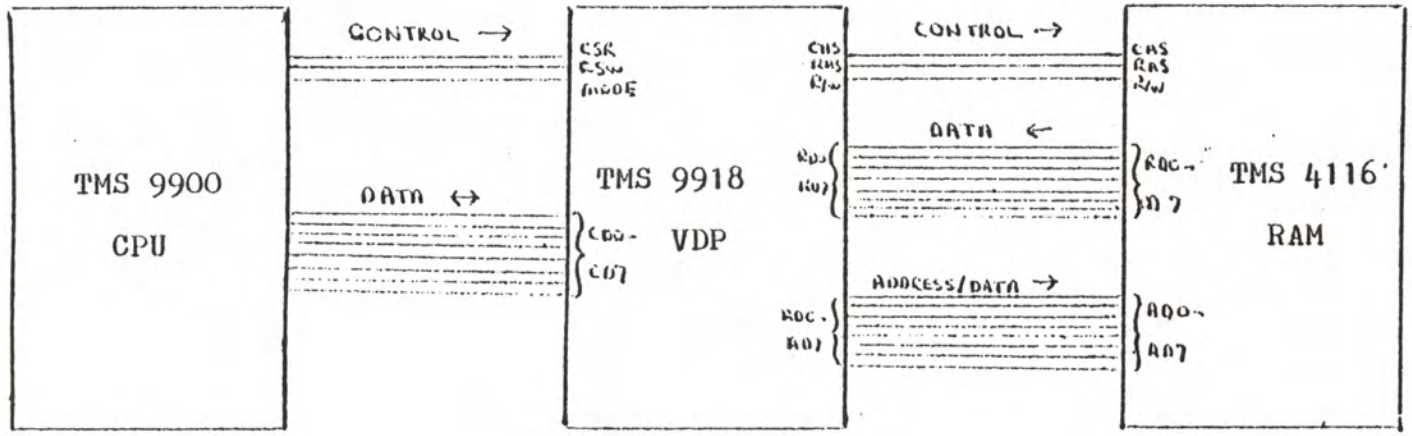


Figure 8. CPU / VDP / RAM Interfacing

PERIPHERALS:

The TI 99/4 Home Computer will be one of the most expandable microprocessor systems when the entire line of peripherals become available. The cassette recorder/player is the only Home Computer accessory that TI will not market, however many types are presently available. Presently the TI 99/4 system is sold with a 13" color moniter. Also available soon will be the following:

* RS 232
* Printer
* Disk Memory Drive
* MODEM
* Solid State Speech Synthesizer
* Plug-In Speech Module
* Command Modules (over sixty presently planned)
* Wired Hand-Held Units (Joysticks)

TABLE 1. Summary of 9900 Microprocessor Instructions

Mnemonic	Instruction Code Description
A	Add Words
AB	Add Bytes
ABS	Absolute Value
AI	Add Immediate
ANDI	AND Immediate
B	Branch
BL	Branch and Link
BLWP	Branch and Load Workspace Pointer
C	Compare Words
CB	Compare Bytes
CI	Compare Immediate
CKOF	Clock off (control instruction)
CKON	Clock on (control instruction)
CLR	CLEAR
COC	Compare Ones Corresponding
CZC	Compare Zeroes Corresponding
DEC	Decrement
DECT	Decrement By Two
DIV	Divide
IDLE	Idle (control instruction)
INC	Increment
INCT	Increment by Two
INV	Invert

Summarry of 9900 Microprocessor Instructions (continued)

Mnemonic	Instruction Code Description
JEQ	Jump If Equal To
JGT	Jump If Greater Than
JH	Jump If Greater Than (Logic)
JHE	Jump If Greater Than Or Equal To (Logic)
JL	Jump If Less Than
JLE	Jump If Less Than Or Equal To (Logic)
JLT	Jump If Less Than
JMP	Unconditioned Jump
JNC	Jump If No Carry
JNE	Jump If Not Equal
JNO	Jump If No Overflow
JOC	Jump On Carry
JOP	Jump On Odd Parity
LDCR	Load CRU
LI	Load Immediate
LIMI	Load Interrupt Mask Immediate
LREX	Restart (control instruction)
LWPI	Load Workspace Pointer Immediate
MOV	Move (word)
MOVB	Move Byte
MPY	Multiply
NEG	Negative
ORI	OR Immediate
RSET	Reset (control instruction)

Summary of 9900 Microprocessor Instructions (continued)

Mnemonic	Instruction Code Description
RTWP	Return with Workspace Pointer
S	Subtract Words
SB	Subtract Bytes
SBO	Set Bit To Logic One
SBZ	Set Bit To Logic Zero
SETO	Set To One
SLA	Shift Left Arithmetic
SOC	Set One Corresponding
SOCB	Set Ones Corresponding Bytes
SRA	Shift Right Arithmetic
SRC	Shift Right Circular
SRL	Shift Right Logical
STCR	Store CRU
STST	Store Status
STWP	Store Workspace Pointer
SWPB	Swap Bytes
SZC	Set To Zeroes Corresponding
SZCB	Set To Zeroes Corresponding Bytes
TB	Test Bit
X	Execute
XOP	Extended Operation
XOR	Exclusive OR

REFERENCES:

1. 9900 Family Systems Design And Data Book; Texas Instruments, Inc. 1978.

2. The TTL Data Book for Design Engineering; Texas Instruments, Inc. 1976.

3. Microprocessor Data Manual; Dave Bursky - Electronic Design, 1978.

4. Microprocessor Interfacing Techniques; Austin Lesea and Rodney Zaks, 1978.

5. Digital Design with Standard MSI and LSI; Thomas R. Blakeslee, 1975.

6. Advanced Circuits - SN76489 Sound Generation Controller; Texas Instruments, Inc. 1978.

7. Electronic News; John Crudde, June 4, 1979.

8. Advanced Circuits - TMS 9918 Video Display Processor, Texas Instruments, Inc. 1978.

PERSONAL COMPUTER REVIEW
HOME COMPUTER
KEY ARCHITECTURAL FEATURES

- 9900 CPU
- VIDEO PROCESSOR WITH 10.74 MHz CRYSTAL OSCILLATOR FOR NTSC COMPOSITE VIDEO GENERATION AND CONTROL OF GRAPHICS RAM
- 3 GRAPHICS ROMS ONBAORD WITH 6K BYTES EACH, EXPANSION PORT FOR SOFTWARE MODULES WITH UP TO FIVE 6K X 8 GROMS AND 8K ROM OR RAM
- 40 KEY KEYBOARD
- TV
- PERIPHERAL CONNECTORS WITH CRU AND 8 BIT MEMORY INTERFACE
- 1200 BAUD HOME CASSETTE INTERFACE

09-26-79 DJH 039-327

TI STRICTLY PRIVATE

PERSONAL COMPUTER REVIEW

HOME COMPUTER

TMS 9918 VIDEO DISPLAY PROCESSOR KEY FEATURES

- REFRESH THE TV SCREEN AT 60 Hz WITHOUT INTERLACE FOR COMPOSITE NTSC VIDEO OUTPUT
- 24 LINES OF 32 CHARACTERS WITH 8 X 8 DOT RESOLUTION
- 32 MOVABLE CHARACTERS WITH MAGNIFICATION
- 24 LINES OF 40 CHARACTERS WITH 6 X 8 DOT RESOLUTION
- 48 LINES OF 64 INDEPENDENT SPOTS
- EXTERNAL VIDEO INPUT WITH SYNC
- PROVIDE 8 COLORS WITH 2 LUMINOUS LEVELS EACH
- PROVIDE 8 SETS OF COLOR SELECT REGISTERS TO PROVIDE SEPARATE COLOR FOR ONES AND ZEROS
- ADDRESS 4-16K BYTES OF RAM FOR CPU OR DISPLAY
- SINGLE 5 VOLT POWER SUPPLY
- 10.74 MHz ONBOARD CRYSTAL OSCILLATOR
- GROM CLOCK
- 40 PIN PLASTIC PACKAGE

PERSONAL COMPUTER REVIEW

HOME COMPUTER

TMC 0430 GRAPHICS ROM KEY FEATURES

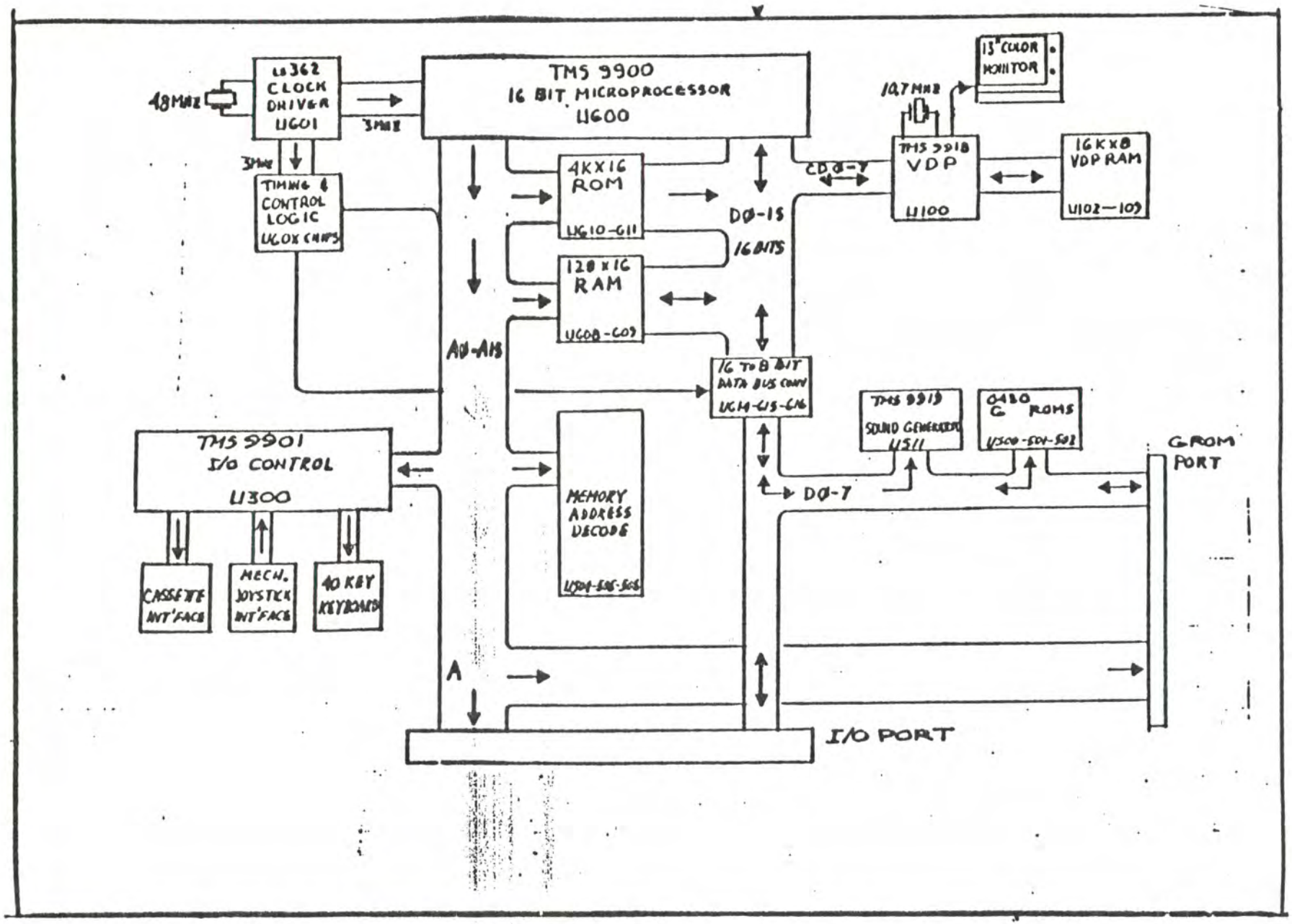
- 6144 BYTES MASK PROGRAMMABLE ROM
- 16 BIT ADDRESS REGISTER WITH INCREMENTER
- CHIP SELECT FROM 3 MOST SIGNIFICANT ADDRESS BITS
- INSTRUCTION DECODE FOR FOUR OPERATIONS
  - READ BYTE AND INCREMENT
  - WRITE HIGH ADDRESS BYTE AND TRANSFER HIGH TO LOW
  - READ LOW ADDRESS BYTE
  - SPARE TO WRITE RAM OR PROM
- LOW COST P CHANNEL MOS
- 9μs CYCLE TIME
- +5, -5 POWER SUPPLIES WITH TTL INTERFACE
- 447.5 KHz CLOCK INPUT
- 16 PIN PACKAGE

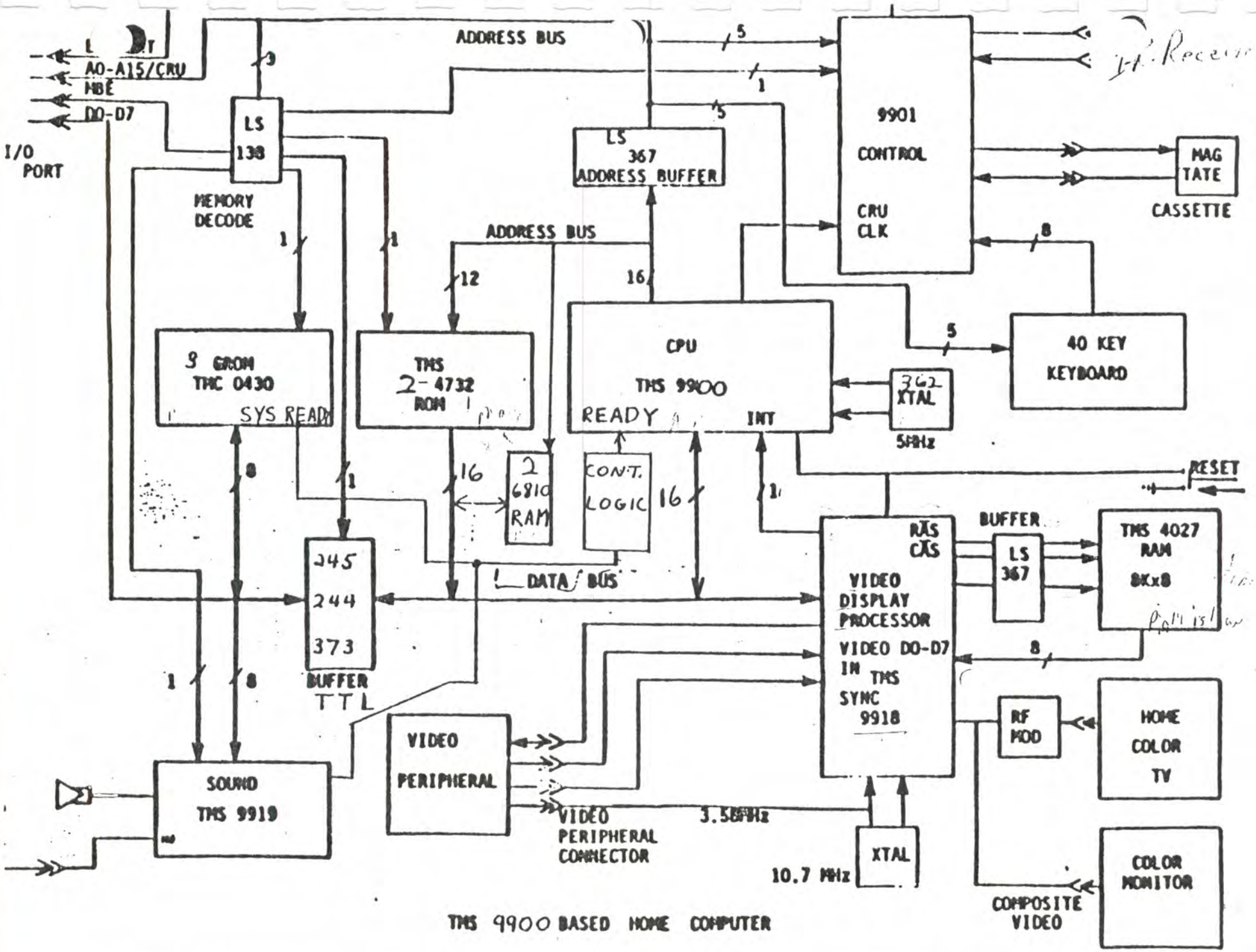
PERSONAL COMPUTER REVIEW

HOME COMPUTER

TIM 9919 SOUND GENERATOR KEY FEATURES

- 3 VOICES WITH 4 OCTAVE MUSICAL RESOLUTION
- 15 BIT PROGRAMMABLE NOISE SHIFT REGISTER
- 100 MW AUDIO DRIVE WITH 30DB CONTROL IN 2DB STEPS
- 8 BIT CPU INTERFACE
- 5V POWER SUPPLY
- I^2L TECHNOLOGY
- 16 PIN PACKAGE


48MHz
LS362
CLOCK
DRIVER
U601
3MHz
3MHz
TMS 9900
16 BIT MICROPROCESSOR
U600
TIMING &
CONTROL
LOGIC
U60X CHIPS
4KX16
ROM
U610-611
128X16
RAM
U608-609
16 BITS
A0-A15
D0-15
10.7MHz
13" COLOR
MONITOR
TMS 9918
VDP
U100
CD 0-7
16KX8
VDP RAM
U102-103
16 TO 8 BIT
DATA BUS CONV
U614-615-616
TMS 9919
SOUND GENERATOR
U511
24K
C ROMS
U500-501-502
GROM
PORT
D0-7
TMS 9901
I/O CONTROL
U300
MEMORY
ADDRESS
DECODE
U604-605-606
CASSETTE
INT'FACE
MECH.
JOYSTICK
INT'FACE
40 KEY
KEYBOARD
A
I/O PORT



THS 9900 BASED HOME COMPUTER

SYSTEM POWER UP

POWER IS TURNED ON:

- 9900 CPU RESETS AND ADDRESSES LOW EPROM LOCATIONS
- 9900 INITIALIZES
- 9900 SETS UP WORKSPACE REGISTERS IN 6810 RAM
- 9900 BEGINS READING FROM GROMS
- 9900 ENTERS TIME DELAY LOOP TO ALLOW STABILIZATION - ¼ SEC
- 9919 SOUND CHIP IS TURNED OFF
- 9918 VDP IS INITIALIZED
- 4027 RAM IS CLEARED - REQUIRES APPROXIMATELY 1 SEC
- FRONT PANEL DISPLAY IS WRITTEN INTO VDP If Dead Press Ready Key + Check signal
- 9919 SOUND CHIP EMITS BEEP
- 9900 CPU ENTERS KEYBOARD SCAN ROUTINE

SYSTEM IS NOW READY FOR USER INPUT

2-13-79 DH

ITEMS TO CHECK DURING DEBUG

1 - CHECK IF FRONT PANEL IS UP "TI LOGO"

2 - CHECK ±5, +12 VOLT LEVELS THROUGHOUT BOARDS

3 - CHECK IF READY PIN 64 OF 9900 IS LOCKED UP

4 - CHECK THE FOUR 12 VOLT CLOCKS FROM 74362 TO 9900

5 - CHECK
  GROM SELECT PIN 10 0430
  GROM READY PIN 15 0430
  GROM CLOCK PIN 13 0430

6 - CHECK PIN 38 OF 9918 FOR 3.579548 MHz CLOCK
  NOTE: SYSTEM WILL RUN WITH CLOCK FROM 3.579520 TO 3.579548 MHz

7 - CHECK VDP (9918) READ PIN 15 9918
  WRITE PIN 14 9918

8 - CHECK DATA OUT OF 4027 RAM PIN 14

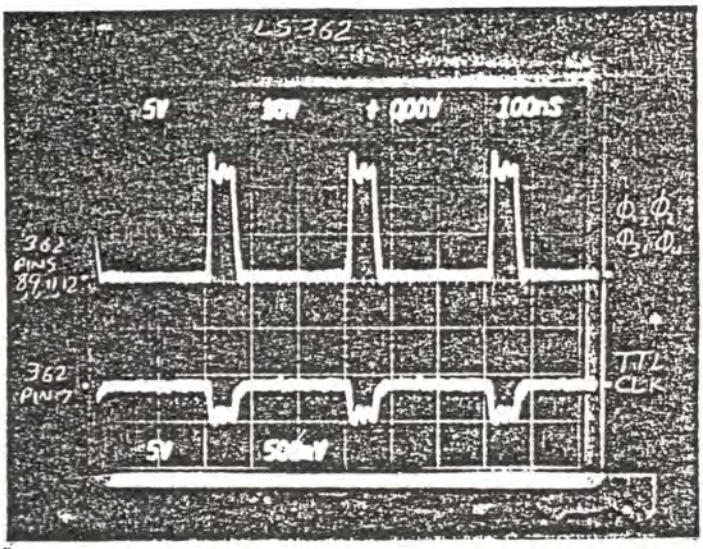
9 - CHECK COMPOSITE VIDEO FROM (BNC CONNECTOR)

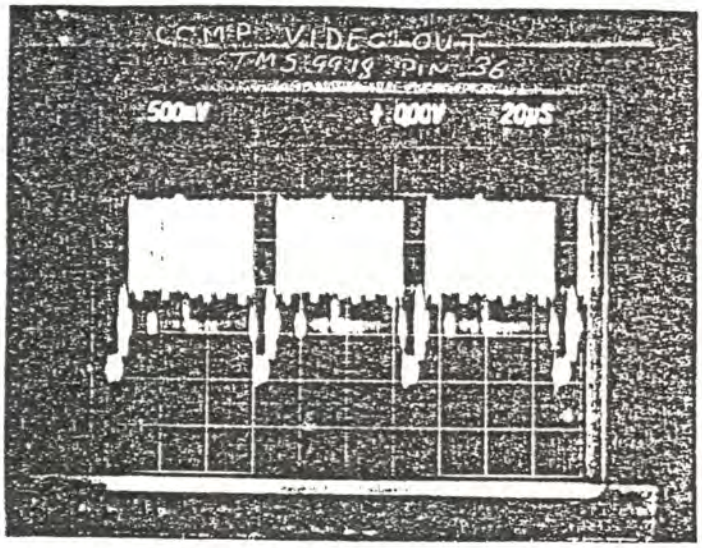
02-14-79 DH

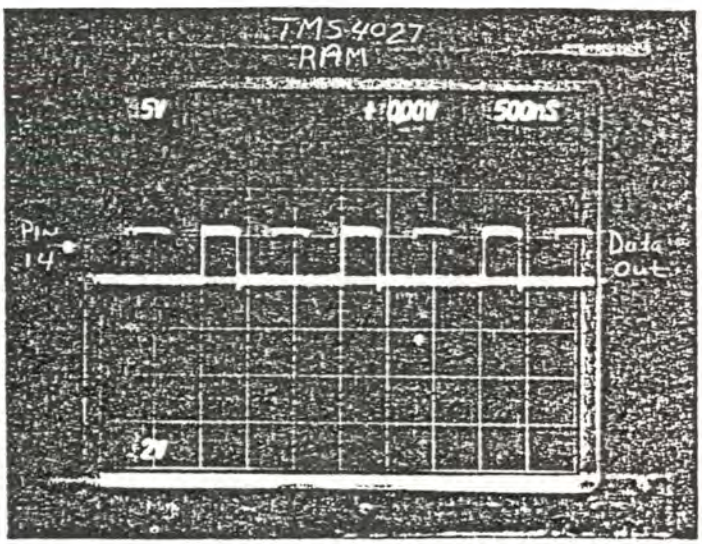
9900 Clock

TTL Clock

Composite VIDEO.





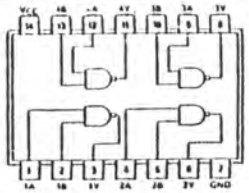


QUADRUPLE 2-INPUT
POSITIVE-NAND GATES

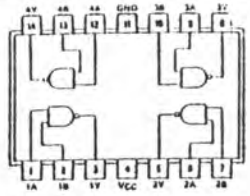
00

positive logic:
$Y = \overline{AB}$

See page 6-2



SN5400 (J) SN7400 (J, N)
SN54H00 (J) SN74H00 (J, N)
SN54L00 (J) SN74L00 (J, N)
SN54LS00 (J, W) SN74LS00 (J, N)
SN54S00 (J, W) SN74S00 (J, N)



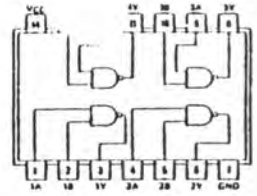
SN5400 (W)
SN54H00 (W)
SN54L00 (T)

QUADRUPLE 2-INPUT
POSITIVE-NAND GATES
WITH OPEN-COLLECTOR OUTPUTS

03

positive logic:
$Y = \overline{AB}$

See page 6-4



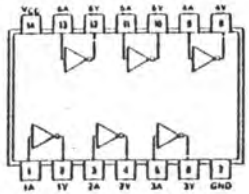
SN5403 (J) SN7403 (J, N)
SN54L03 (J) SN74L03 (J, N)
SN54LS03 (J, W) SN74LS03 (J, N)
SN54S03 (J, W) SN74S03 (J, N)

HEX INVERTERS

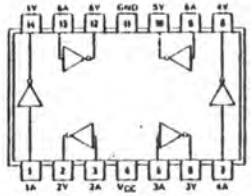
04

positive logic:
$Y = \overline{A}$

See page 6-2



SN5404 (J) SN7404 (J, N)
SN54H04 (J) SN74H04 (J, N)
SN54L04 (J) SN74L04 (J, N)
SN54LS04 (J, W) SN74LS04 (J, N)
SN54S04 (J, W) SN74S04 (J, N)



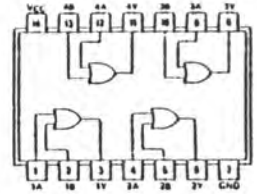
SN5404 (W)
SN54H04 (W)
SN54L04 (T)

QUADRUPLE 2-INPUT
POSITIVE-OR GATES

32

positive logic:
$Y = A+B$

See page 6-28



SN5432 (J, W) SN7432 (J, N)
SN54LS32 (J, W) SN74LS32 (J, N)
SN54S32 (J, W) SN74S32 (J, N)

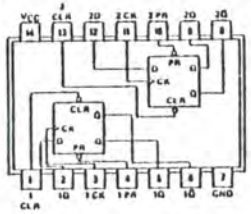
DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

74

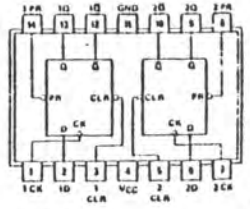
FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$

See pages 6-46, 6-50, 6-54, and 6-56



SN5474 (J) SN7474 (J, N)
SN54H74 (J) SN74H74 (J, N)
SN54L74 (J) SN74L74 (J, N)
SN54LS74A (J, W) SN74LS74A (J, N)
SN54S74 (J, W) SN74S74 (J, N)



SN5474 (W)
SN54H74 (W)
SN54L74 (T)

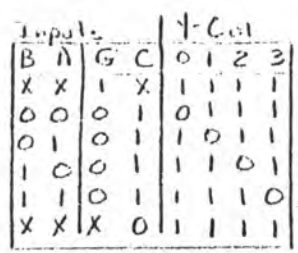
DECODERS/DEMULTIPLEXERS

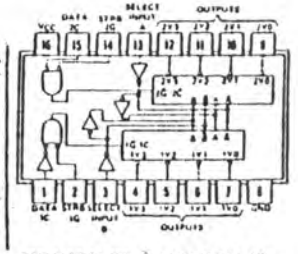
DUAL 2- TO 4-LINE DECODER
DUAL 1- TO 4-LINE DEMULTIPLEXER
3- TO 8-LINE DECODER
1- TO 8-LINE DEMULTIPLEXER

155 TOTEM-POLE OUTPUTS

156 OPEN-COLLECTOR OUTPUTS

See page 7-175



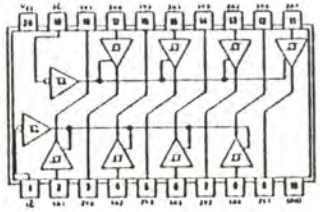


SN54155 (J, W) SN74155 (J, N)
SN54LS155 (J, W) SN74LS155 (J, N)
SN54156 (J, W) SN74156 (J, N)
SN54LS156 (J, W) SN74LS156 (J, N)

OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS

244 NONINVERTED 3-STATE OUTPUTS

See page 6-83

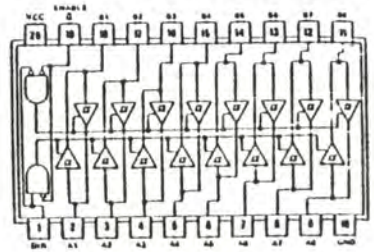


SN54LS244 (J) SN74LS244 (J, N)

OCTAL BUS TRANCEIVERS

245 NONINVERTED 3-STATE OUTPUTS

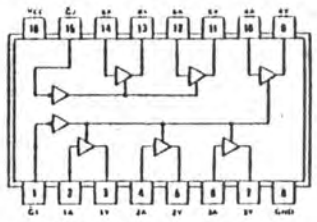
See page 7-349



SN54LS245 (J) SN74LS245 (J, N)

HEX BUS DRIVERS

367 NONINVERTED DATA OUTPUT
4-LINE AND 2-LINE ENABLE INPUTS
3-STATE OUTPUTS

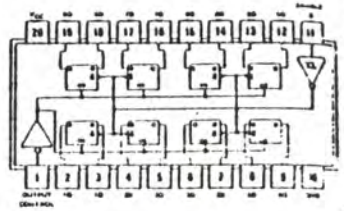


SN54367A (J, W) SN74367A (J, N)
SN54LS367 (J, W) SN74LS367 (J, N)

See page 6-36

OCTAL D-TYPE LATCHES

373 3-STATE OUTPUTS
COMMON OUTPUT CONTROL
COMMON ENABLE

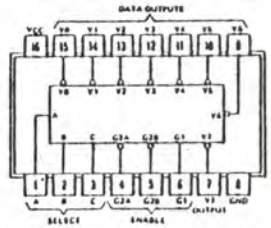


SN54LS373 (J) SN74LS373 (J, N)
SN54S373 (J) SN74S373 (J, N)

See page 7-471

3-TO-8 LINE DECODERS/MULTIPLEXERS

138



SN54LS138 (J, W) SN74LS138 (J, N)
SN54S138 (J, W) SN74S138 (J, N)

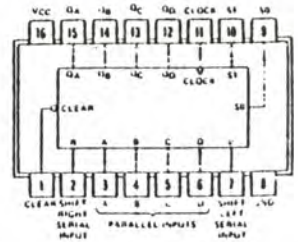
See page 7-134

74LS138

Inputs					Y - Outputs							
Enable		Select										
G1	G2*	C	B	A	0	1	2	3	4	5	6	7
X	1	X	X	X	1	1	1	1	1	1	1	1
0	X	X	X	X	1	1	1	1	1	1	1	1
1	0	0	0	0	0	1	1	1	1	1	1	1
1	0	0	0	1	1	0	1	1	1	1	1	1
1	0	0	1	0	1	1	0	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1	1	1
1	0	1	0	0	1	1	1	1	0	1	1	1
1	0	1	0	1	1	1	1	1	1	0	1	1
1	0	1	1	0	1	1	1	1	1	1	0	1
1	0	1	1	1	1	1	1	1	1	1	1	0

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

194



SN54194 (J, W) SN74194 (J, N)
SN54LS194A (J, W) SN74LS194A (J, N)
SN54S194 (J, W) SN74S194 (J, N)

See page 7-316

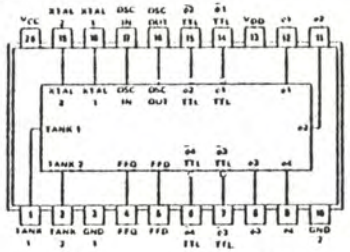
74LS194

	Mode		Serial		Parallel				Outputs			
Clear	S_1	S_0	Left	Right	A	B	C	D	Q_A	Q_B	Q_C	Q_D
0	X	X	X	X	X	X	X	X	L	L	L	L
1	X	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
1	1	1	X	X	a	b	c	d	a	b	c	d
1	1	0	X	1	X	X	X	X	1	Q_{An}	Q_{Bn}	Q_{Cn}
1	0	1	X	0	X	X	X	X	0	Q_{An}	Q_{Bn}	Q_{Cn}
1	0	0	1	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	1
1	0	0	0	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	0
1	1	0	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

Modes- S_0 S_1
0 0 - Do Nothing
0 1 - Shift Left
1 0 - Shift Right
1 1 - Parallel

FOUR PHASE CI NERATOR/DRIVER
FOR TMS 9900 F ROCESSOR

362



See page 7-460

SN74LS362 (J, N)

PARAMETER MEASUREMENT INFORMATION

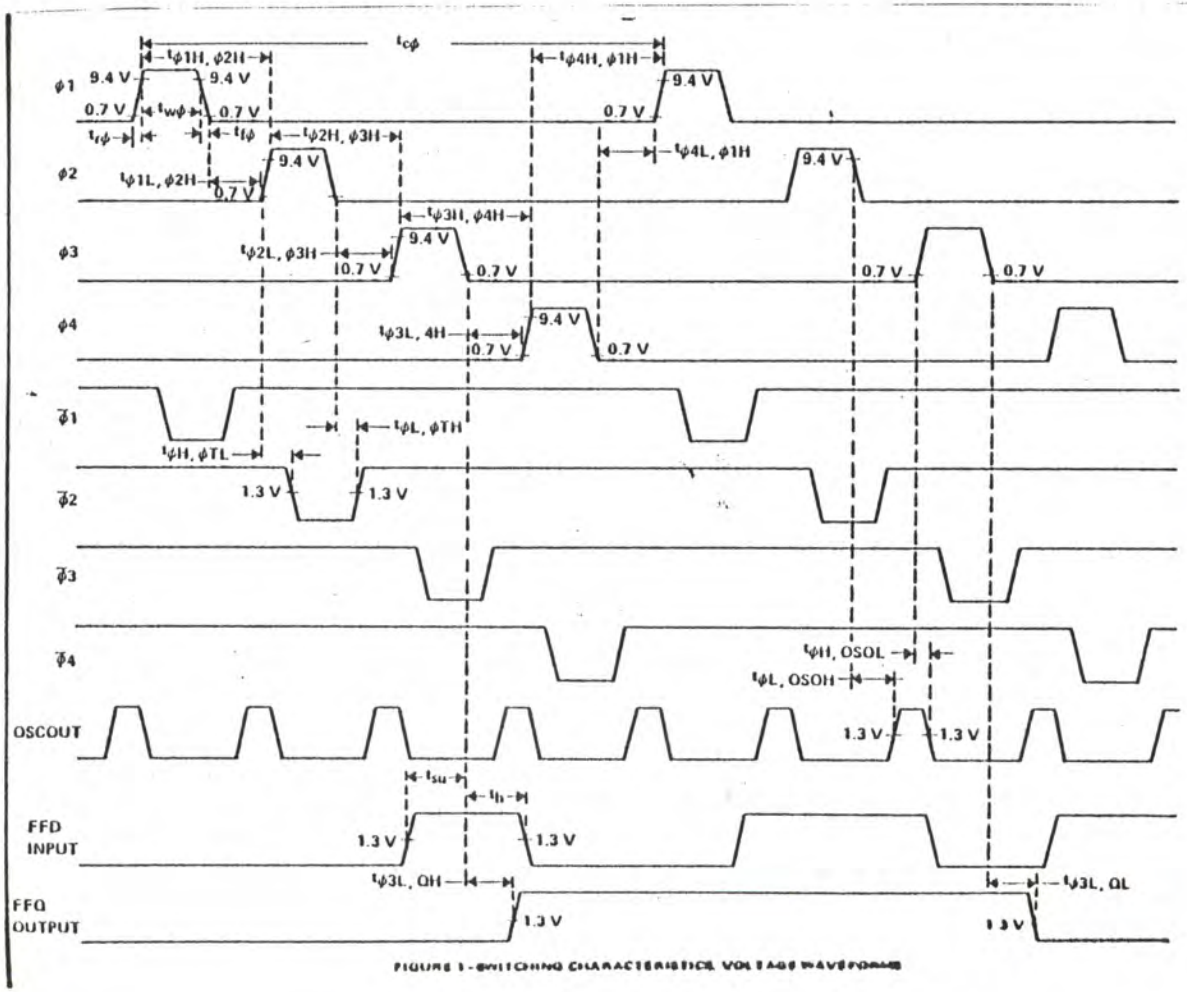


FIGURE 1-SWITCHING CHARACTERISTICS, VOLTAGE WAVEFORMS

TMS 9900 PIN ASSIGNMENTS

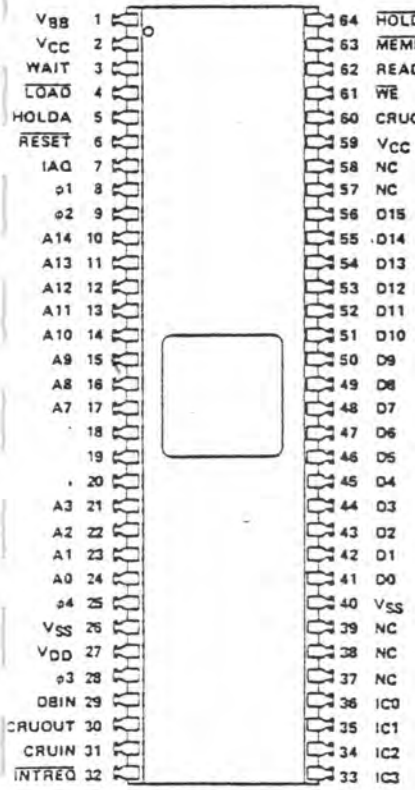


TABLE 2 (CONTINUED)

SIGNATURE	PIN	I/O	DESCRIPTION
			BUS CONTROL
DBIN	29	OUT	Data bus in. When active (high), DBIN indicates that the TMS 9900 has disabled its output buffers to allow the memory to place memory-read data on the data bus during $\overline{\text{MEMEN}}$. DBIN remains low in all other cases except when HOLDA is active.
$\overline{\text{MEMEN}}$	63	OUT	Memory enable. When active (low), $\overline{\text{MEMEN}}$ indicates that the address bus contains a memory address.
$\overline{\text{WE}}$	61	OUT	Write enable. When active (low), $\overline{\text{WE}}$ indicates that memory-write data is available from the TMS 9900 to be written into memory.
CRUCLK	60	OUT	CRU clock. When active (high), CRUCLK indicates that external interface logic should sample the output data on CRUOUT or should decode external instructions on A0 through A2.
CRUIN	31	IN	CRU data in. CRUIN, normally driven by 3-state or open-collector devices, receives input data from external interface logic. When the processor executes a STCR or TB instruction, it samples CRUIN for the level of the CRU input bit specified by the address bus (A3 through A14).
CRUOUT	30	OUT	CRU data out. Serial I/O data appears on the CRUOUT line when an LDCR, SBZ, or SBO instruction is executed. The data on CRUOUT should be sampled by external I/O interface logic when CRUCLK goes active (high).
			INTERRUPT CONTROL
$\overline{\text{INTREQ}}$	32	IN	Interrupt request. When active (low), $\overline{\text{INTREQ}}$ indicates that an external interrupt is requested. If $\overline{\text{INTREQ}}$ is active, the processor loads the data on the interrupt-code-input lines IC0 through IC3 into the internal interrupt-code-storage register. The code is compared to the interrupt mask bits of the status register. If equal or higher priority than the enabled interrupt level (interrupt code equal or less than status register bits 12 through 15) the TMS 9900 interrupt sequence is initiated. If the comparison fails, the processor ignores the request. $\overline{\text{INTREQ}}$ should remain active and the processor will continue to sample IC0 through IC3 until the program enables a sufficiently low priority to accept the request interrupt.
IC0 (MSB)	36	IN	Interrupt codes. IC0 is the MSB of the interrupt code, which is sampled when $\overline{\text{INTREQ}}$ is active. When IC0 through IC3 are LLLH, the highest external-priority interrupt is being requested and when HHHH, the lowest-priority interrupt is being requested.
IC1	35	IN	
IC2	34	IN	
IC3 (LSB)	33	IN	
			MEMORY CONTROL
$\overline{\text{HOLD}}$	64	IN	Hold. When active (low), $\overline{\text{HOLD}}$ indicates to the processor that an external controller (e.g., DMA device) desires to utilize the address and data buses to transfer data to or from memory. The TMS 9900 enters the hold state following a hold signal when it has completed its present memory cycle.* The processor then places the address and data buses in the high-impedance state (along with $\overline{\text{WE}}$, $\overline{\text{MEMEN}}$, and DBIN) and responds with a hold-acknowledge signal (HOLDA). When $\overline{\text{HOLD}}$ is removed, the processor returns to normal operation.
HOLDA	5	OUT	Hold acknowledge. When active (high), HOLDA indicates that the processor is in the hold state and the address and data buses and memory control outputs ($\overline{\text{WE}}$, $\overline{\text{MEMEN}}$, and DBIN) are in the high-impedance state.
READY	62	IN	Ready. When active (high), READY indicates that memory will be ready to read or write during the next clock cycle. When not-ready is indicated during a memory operation, the TMS 9900 enters a wait state and suspends internal operation until the memory systems indicate ready.
WAIT	3	OUT	Wait. When active (high), WAIT indicates that the TMS 9900 has entered a wait state because of a not-ready condition from memory.

*If the cycle following the present memory cycle is also a memory cycle, it, too, is completed before the TMS9900 enters the hold state. The maximum number of consecutive memory cycles is three.

TABLE 2 (CONCLUDED)

SIGNATURE	PIN	I/O	DESCRIPTION
			TIMING AND CONTROL
IAQ	7	OUT	Instruction acquisition. IAQ is active (high) during any memory cycle when the TMS 9900 is acquiring an instruction. IAQ can be used to detect illegal op codes.
$\overline{\text{LOAD}}$	4	IN	Load. When active (low), $\overline{\text{LOAD}}$ causes the TMS 9900 to execute a nonmaskable interrupt with memory address FFFC_{16} containing the trap vector (WP and PC). The load sequence begins after the instruction being executed is completed. $\overline{\text{LOAD}}$ will also terminate an idle state. If $\overline{\text{LOAD}}$ is active during the time $\overline{\text{RESET}}$ is released, then the $\overline{\text{LOAD}}$ trap will occur after the $\overline{\text{RESET}}$ function is completed. $\overline{\text{LOAD}}$ should remain active for one instruction period. IAQ can be used to determine instruction boundaries. This signal can be used to implement cold-start ROM loaders. Additionally, front-panel routines can be implemented using CRU bits as front-panel-interface signals and software-control routines to control the panel operations.
$\overline{\text{RESET}}$	6	IN	Reset. When active (low), $\overline{\text{RESET}}$ causes the processor to be reset and inhibits $\overline{\text{WE}}$ and CRUCLK. When $\overline{\text{RESET}}$ is released, the TMS 9900 then initiates a level-zero interrupt sequence that acquires WP and PC from locations 0000 and 0002, sets all status register bits to zero, and starts execution. $\overline{\text{RESET}}$ will also terminate an idle state. $\overline{\text{RESET}}$ must be held active for a minimum of three clock cycles.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage	FFD					0.5	V
		OSCIN					0.8	
$V_{T+} - V_{T-}$	Hysteresis	FFD			0.4	0.8		V
V_{IK}	Input clamp voltage		V_{CC} = 4.75 V, V_{DD} = 11.4 V, I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	ϕ1, ϕ2, ϕ3, ϕ4	V_{CC} = 4.75 V,	I_{OH} = −100 μA	V_{DD}−2	V_{DD}−1.5	V_{DD}	V
		Other outputs	V_{DD} = 11.4 V to 12.6 V	I_{OH} = −400 μA	2.7	3.4		
V_{OL}	Low-level output voltage	ϕ1, ϕ2, ϕ3, ϕ4	V_{CC} = 4.75 V, V_{DD} = 11.4 V	I_{OL} = 4 mA		0.25	0.4	mA
		Other outputs		I_{OL} = 4 mA		0.25	0.4	
				I_{OL} = 8 mA		0.35	0.5	
I_I	Input current at maximum input voltage	FFD	V_{CC} = 5.25 V, V_{DD} = 12.6 V	V_I = 7 V			0.1	mA
		OSCIN		V_I = 5.5 V			0.3	
I_{IH}	High-level input current	FFD	V_{CC} = 5.25 V, V_{DD} = 12.6 V, V_I = 2.7 V				20	μA
		OSCIN					60	
I_{IL}	Low-level input current	FFD	V_{CC} = 5.25 V, V_{DD} = 12.6 V, V_I = 0.4 V				−0.4	mA
		OSCIN					−3.2	
I_{OS}	Short-circuit output current‡	All except ϕ1, ϕ2, ϕ3, ϕ4	V_{CC} = 5.25 V		−20		−100	mA
I_{CC}	Supply current from V_{CC}		V_{CC} = 5.25 V, FFD and OSCIN at GND, Outputs open			105	175	mA
I_{DD}	Supply current from V_{DD}		V_{CC} = 5.25 V, V_{DD} = 12.6 V, FFD and OSCIN at GND, Outputs open			12	20	mA

†All typical values are at V_{CC} = 5 V, V_{DD} = 12 V, T_A = 25°C.
‡Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second. Outputs ϕ1, ϕ2, ϕ3, and ϕ4 do not have short-circuit protection.

switching characteristics, T_A = 25°C, V_{CC1} = 5 V, V_{CC2} = 12 V, f_{osc} = 48 MHz, see figure 1

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{out}	Output frequency, any ϕ or $\bar{\phi}$ TTL	Output loads: ϕ1, ϕ3, ϕ4: 100 pF to GND; ϕ2: 200 pF to GND; Others: R_L = 2 kΩ, C_L = 15 pF; See Note 2		3		MHz
f_{out}	Output frequency, OSCOUT			12		MHz
$t_{c(\phi)}$	Cycle time, any ϕ output			333		ns
$t_{r(\phi)}$	Rise time, any ϕ output		10		20	ns
$t_{f(\phi)}$	Fall time, any ϕ output		10		20	ns
$t_{w(\phi)}$	Pulse width, any ϕ output high		40			ns
$t_{\phi1L,\phi2H}$	Delay time, ϕ1 low to ϕ2 high		0	5	15	ns
$t_{\phi2L,\phi3H}$	Delay time, ϕ2 low to ϕ3 high		0	5	15	ns
$t_{\phi3L,\phi4H}$	Delay time, ϕ3 low to ϕ4 high		0	5	15	ns
$t_{\phi4L,\phi1H}$	Delay time, ϕ4 low to ϕ1 high		0	5	15	ns
$t_{\phi1H,\phi2H}$	Delay time, ϕ1 high to ϕ2 high		70	83		ns
$t_{\phi2H,\phi3H}$	Delay time, ϕ2 high to ϕ3 high		70	83		ns
$t_{\phi3H,\phi4H}$	Delay time, ϕ3 high to ϕ4 high		70	83		ns
$t_{\phi4H,\phi1H}$	Delay time, ϕ4 high to ϕ1 high		70	83		ns
$t_{\phi H,\bar{\phi}TL}$	Delay time, ϕ_n high to $\bar{\phi}_n$ TTL low			−8		ns
$t_{\phi L,\bar{\phi}TH}$	Delay time, ϕ_n low to $\bar{\phi}_n$ TTL high			−19		ns
$t_{\phi3L,QH}$	Delay time, ϕ3 low to FFQ output high			−7		ns
$t_{\phi3L,QL}$	Delay time, ϕ3 low to FFQ output low			−12		ns
$t_{\phi L,OSOH}$	Delay time, ϕ low to OSCOUT high			−5		ns
$t_{\phi H,OSOL}$	Delay time, FFQ high to OSCOUT low			−13		ns

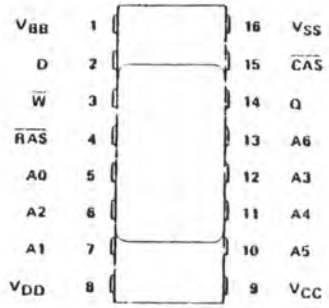
NOTE 2: Use load circuit for bi-state totem-pole outputs, page 3-11.

- 16,384 X 1 Organization
- 10% Tolerance on All Supplies
- All Inputs Including Clocks TTL-Compatible
- Unlatched Three-State Fully TTL-Compatible Output
- 3 Performance Ranges:

	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ, MODIFY-WRITE† CYCLE (MIN)
TMS 4116-15	150 ns	100 ns	375 ns	375 ns
TMS 4116-20	200 ns	135 ns	375 ns	375 ns
TMS 4116-25	250 ns	165 ns	410 ns	515 ns

- Page-Mode Operation for Faster Access Time
- Common I/O Capability with "Early Write" Feature
- Low-Power Dissipation
  - Operating 462 mW (max)
  - Standby 20 mW (max)
- 1-T Cell Design, N-Channel Silicon-Gate Technology
- 16-Pin 300-Mil (7.62 mm) Package Configuration

16-PIN CERAMIC AND PLASTIC DUAL-IN-LINE PACKAGES
(TOP VIEW)



PIN NOMENCLATURE			
A0-A6	Address Inputs	W	Write Enable
CAS	Column address strobe	VBB	−5-V power supply
D	Data input	VCC	+5-V power supply
Q	Data output	VDD	+12-V power supply
RAS	Row address strobe	VSS	0 V ground

ription

The TMS 4116 JL series is composed of monolithic high-speed dynamic 16,384-bit MOS random-access memories is organized as 16,384 one-bit words, and employs single-transistor storage cells and N-channel silicon-gate technology.

All inputs and outputs are compatible with Series 74 TTL circuits including clocks: Row Address Strobe RAS (or R) and Column Address Strobe CAS (or C). All address lines (A0 through A6) and data-in (D) are latched on chip to simplify system design. Data out (Q) is unlatched to allow greater system flexibility.

Typical power dissipation is less than 350 milliwatts active and 6 milliwatts during standby (V_{CC} is not required during standby operation). To retain data, only 10 milliwatts average power is required which includes the power consumed to refresh the contents of the memory.

The TMS 4116 series is offered in 16-pin dual-in-line cerdip (JL suffix), sidebraze (JDL suffix), and plastic (NL suffix) packages and is guaranteed for operation from 0°C to 70°C. Packages are designed for insertion in mounting-hole rows on 300 mil (7.62 mm) centers.

ration

address (A0 through A6)

Fourteen address bits are required to decode 1 of 16,384 storage cell locations. Seven row-address bits are set up on pins A0 through A6 and latched onto the chip by the row-address strobe (RAS). Then the seven column-address bits are set up on pins A0 through A6 and latched onto the chip by the column-address strobe (CAS). All addresses must be stable on or before the falling edges of RAS and CAS. RAS is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. CAS is used as a chip select activating the column decoder and the input and output buffers.

erm "read write cycle" is sometimes used as an alternative title to "read modify write cycle".

write enable (W)

The read or write mode is selected through the write enable (W) input. A logic high on the W input selects the rea mode and a logic low selects the write mode. The write enable terminal can be driven from standard TTL circui without a pull-up resistor. The data input is disabled when the read mode is selected. When W goes low prior to CA data out will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data-in (D)

Data is written during a write or read-modify write cycle. The latter falling edge of CAS or W strobes data into th on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early writ cycle W is brought low prior to CAS and the data is strobed in by CAS with setup and hold times referenced to th signal. In a delayed write or read-modify write cycle, CAS will already be low, thus the data will be strobed in by t with setup and hold times referenced to this signal.

data-out (Q)

The three state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan-out of tw Series 74 TTL loads. Data-out is the same polarity as data-in. The output is in the high-impedance (floating) state unt CAS is brought low. In a read cycle the output goes active after the enable time interval $t_{a(C)}$ that begins with th negative transition of CAS as long as $t_{a(R)}$ is satisfied. The output becomes valid after the access time has elapsed an remains valid while CAS is low; CAS going high returns it to a high-impedance state. In an early write cycle, the outpu is always in the high-impedance state. In a delayed write or read-modify-write cycle, the output will follow th sequence for the read cycle.

refresh

A refresh operation must be performed at least every two milliseconds to retain data. Since the output buffer is in th high-impedance state unless CAS is applied, the RAS only refresh sequence avoids any output during refresh. Strobin each of the 128 row addresses (A0 through A6) with RAS causes all bits in each row to be refreshed. CAS remains hig (inactive) for this refresh sequence, thus conserving power.

page mode

Page mode operation allows effectively faster memory access by keeping the same row address and strobing successiv column addresses onto the chip. Thus, the time required to setup and strobe sequential row addresses on the same pag is eliminated. To extend beyond the 128 column locations on a single RAM, the row address and RAS is applied t multiple 16K RAMs CAS is decoded to select the proper RAM.

power-up

V_{BB} must be applied to the device either before or at the same time as the other supplies and removed last. Failure t observe this precaution will cause dissipation in excess of the absolute maximum ratings due to internal forward bia conditions. This also applies to system use, where failure of the V_{BB} supply must immediately shut down the othe supplies. After power up, eight memory cycles must be performed to achieve proper device operation.

COURSE OUTLINE

Color Theory

Bill Rich

First Section, 2 Hours, Mr. Rich

Colorimetry

Make-up of the color picture signal
- Development of Subcarrier Frequency
- Color Synchronization
- Chrominance signals
- Vector relationship of color signals

Second Section, 1 1/2 Hour, Mr. Rich

Block diagram of the color section of a Color TV

Color Picture Tube and Associated Circuits
- Focus grid
- Screen grid and controls
- Control grid
- Cathode
- Bias
- Drive controls-tracking

Third Section, 2 Hours, Mr. Hawkins

Chrominance Section
- Bandpass amplifier
- Chroma Output
- Automatic Chroma Control (ACC)
- Color Killer

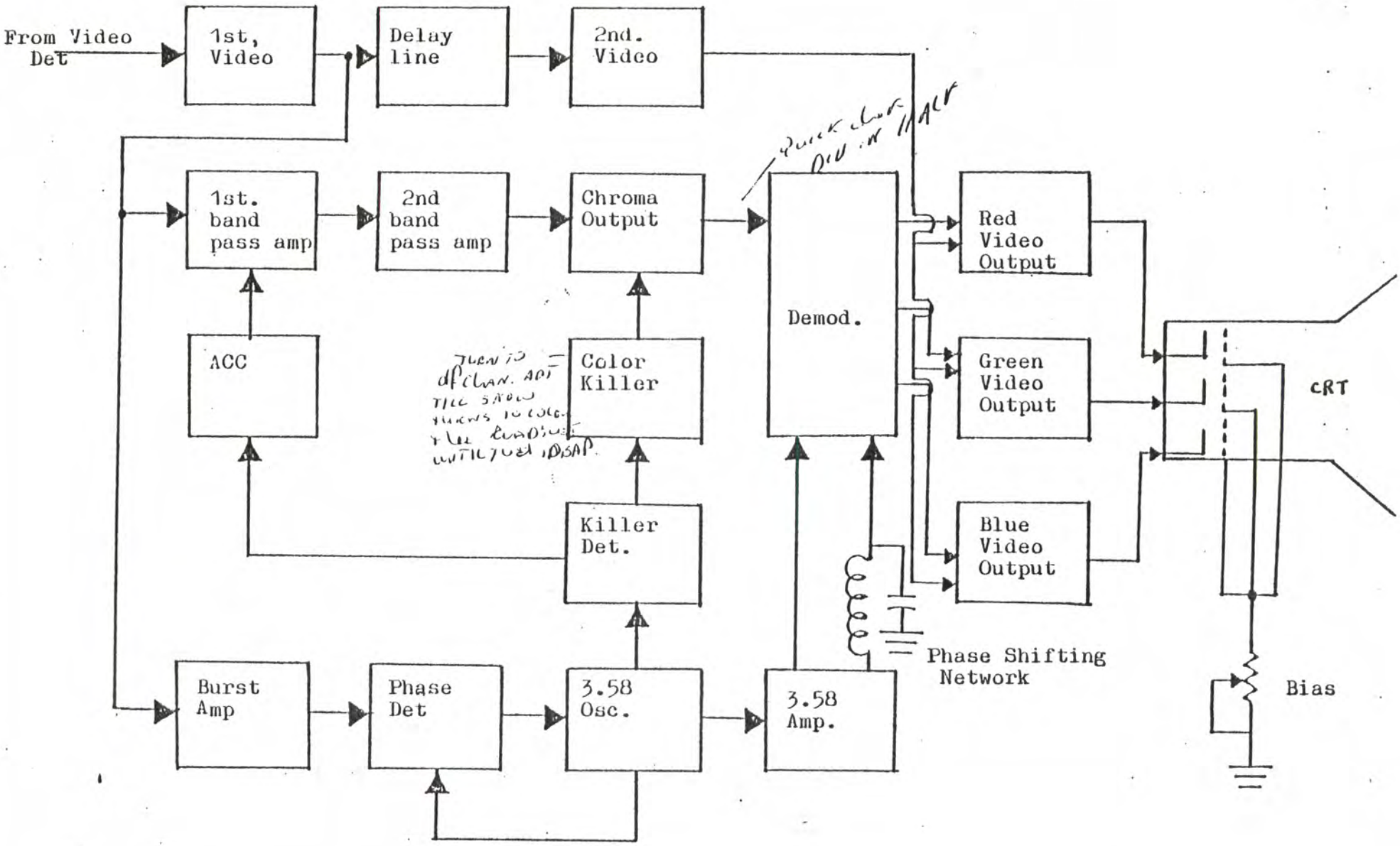
Color Sync
- Burst Amp.
- 3.58 Oscillator
- 3.58 Amp.
- C. W. Signals
- Phase Splitter

Fourth Section, 1 ½ Hour, Mr. Hawkins

Color demodulation
- Bipolar transistor demodulation
- Diode demodulation
- IC demodulation

Matrix (Mixing of Chrominance and Luminance)

Red video output
Blue video output
Green video output


From Video Det
1st, Video
Delay line
2nd. Video
1st. band pass amp
2nd band pass amp
Chroma Output
Demod.
Red Video Output
Green Video Output
Blue Video Output
CRT
ACC
Color Killer
Killer Det.
Burst Amp
Phase Det
3.58 Osc.
3.58 Amp.
Phase Shifting Network
Bias

THE OPERATION OF THE COLOR PORTION OF A COLOR TELEVISION

The input to the color circuitry is derived from the video detector. This video signal passes to two stages. The upper stage is the band pass amplifier, whose function is to extract only the color information from the composite video signal. The output of this stage therefore, has present only 3.58 megacycle color information. There is not sync or black and white information present at this point. The output of the band pass amplifier is then fed to the chroma demodulators.

The output of the demodulators in turn feed the base of the red, blue, and green output transistors. The Y signal is then fed into the red, blue and green video output emitters. The Y signal is the black and white or brightness (luminance) signal.

The signals of the red video output is then injected into the red cathodes of the picture tube. The green output into the green cathode and the blue output into the blue cathode of the CRT. The signals of the red, blue and green outputs are then injected into their respective red, blue and green cathodes of the picture tube. The net affect to the picture tube is that the red video is converted into a red picture which represents the original red information in the transmitted picture and the blue signal that is applied to the blue cathode represents the blue of the original transmitted picture and the same situation applies to the green video output stage.

Since the color signal fed to the demodulators consists of side bands only, we must reinsert a carrier, in order to properly demodulate or detect. This carrier must not only be of the correct frequency, but must also be of the proper phase. The reinjected carrier is supplied by the 3.58 oscillator in the receiver

and you will note that one half of the demodulator receives its signal directly from the junction of L and C, a phase shift network. This network provides the necessary phase shift in order to demodulate at the correct angles.

Since the 3.58 oscillator is crystal controlled, this partially takes care of the frequency requirements. In order to maintain the proper phase of the carrier, this oscillator is in turn compared to the original transmitted signal and phase locked. The net result is that the output of the 3.58 oscillator in the receiver is of precisely the same frequency and precisely the same phase as the original transmitted burst or reference signal.

This is accomplished when the signal from the video detector not only feeds the band pass amplifier, but also feeds the burst amplifier. The burst signal is contained on the back porch of the horizontal sync pulse of the transmitted signal. The burst amplifier is turned on by means of a high level pulse from the horizontal flyback system of the receiver. The output of the burst amplifier, therefore, consists only of information present during the horizontal blanking period, which is the burst signal. This burst signal is fed to a phase detector which it is compared with a sample of the RF signal from the 3.58 oscillator in the receiver. If there is a difference in frequency or phase a correction voltage is developed which feeds the bias network of the 3.58 oscillator which in turn restores the 3.58 oscillator in the receiver to the proper frequency and phase.

We will now determine the contribution of each of these stages to the performance of a color set. If the band pass amplifier or 3.58 oscillator where inoperative, no color information would be present on the face of the kinescope, but it would not be synchronized, and you would find the color running through the picture in a manner similar to an out of sync horizontal condition. Black and white would remain in sync and appear perfectly normal, but the color would be randomly floating through the picture. We can conclude that at any time that

we have an out of sync color condition, that the trouble must lie in the burst amplifier, the phase detector or the 3.58 oscillator.

If either of the demodulators are not working properly or are totally inoperative, this would result in no output or improper output from the particular demodulator. If one half of the demodulator were not working properly we would see no red. If the other half were inoperative, we would see no blue. The red, blue and green video output transistors matrix and amplify the chrominance and the luminance signals. They also control the cathode bias on the picture tube. If all of the outputs stop conducting at the same time the picture tube will be biased off, and will not produce a raster (brightness). If they over conduct brightness will be excessive and the brightness control may not affect the raster. If only one video output quits conducting or over conducts the brightness will only be affected in that specific color.

The red, blue and green video stages must have uniform gain to produce good color tracking. This is usually accomplished with bias and drive controls to each video output stage.

COLOR KILLER AND AUTOMATIC CHROMA CONTROL (ACC)

For a monochrome picture, the color receiver uses only the amplifiers for Y luminance signal. The 3.58-MHz chroma bandpass amplifier and chroma demodulators are not needed because there is no color signal to amplify. When the 3.58-MHz color circuits are on without any signal applied, they generate receiver noise. This appears in the picture as color snow or "confetti." In a monochrome picture, crosstalk between the color snow and high-frequency components of the luminance signal produces color sparkle at the edges of black-and-white objects in the scene.

The function of the color killer is to cut off the 3.58-MHz chroma circuits when there is no color signal. Either the bandpass amplifier or the demodulators can be turned off by the color killer. A threshold or level control is provided

to adjust the point where the killer circuit automatically cuts off the chroma circuits for a black-and-white program.

The color killer circuit recognizes a monochrome program by the absence of the color burst signal. Any time there is no separated burst for color synchronization, the color killer will cut off the color amplifier.

Automatic chroma control (ACC) is to the chroma bandpass amplifier as the AGC bias circuit is the picture IF amplifier. The ACC bias varies the gain for the 3.58-MHz bandpass amplifier inversely as the strength of the received color signal. The signal strength is determined from the relative amplitude of burst. More burst means more color signal, which needs less gain in the bandpass amplifier. As a result, the ACC circuit maintains a constant color level in the picture when changing stations.

The color killer and ACC circuits usually function together. The reason is that they both depend on the 3.58-MHz color sync burst transmitted on the back porch of the horizontal blanking pulses. Burst amplitude determines the ACC bias. No burst at all means the color killer operates to cut off the color amplifier.

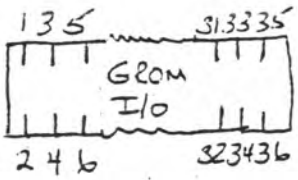
The amount of 3.58-MHz oscillator cw input to the killer detector depends on the burst input to the oscillator. The detector rectifies this ac input to produce a dc bias voltage. For the killer, the bias is amplified to cut off the second bandpass amplifier. For the ACC circuit, the bias is amplified to control the gain of the first bandpass amplifier.

2000

1	EARLY LEARNING
2	EARLY LEARNING
3	MAINFRAME
4	MAINFRAME
5	MAINFRAME
6	DIAGNOSTIC
7	EXERCISE PHYSICAL FITNESS
8	EXERCISE PHYSICAL FITNESS
9	FOOTBALL
10	FOOTBALL
11	NUMBER MAGIC
12	GRAMMAR
13	GRAMMAR
14	GRAMMAR
15	HOUSEHOLD BUDGET
16	HOUSEHOLD BUDGET
17	HOME FINANCIAL DECISIONS
18	HOME FINANCIAL DECISIONS
19	VIDEO GRAPH
20	VIDEO CHESS
21	VIDEO CHESS
22	VIDEO CHESS
23	VIDEO CHESS
24	DEMO
25	DEMO
26	DEMO
27	DEMO
28	PRE-SCHOOL U.K.
29	PRE-SCHOOL U.K.
30	HOUSEHOLD BUDGET U.K.
31	HOUSEHOLD BUDGET U.K.
32	SPEECH EDITOR
33	Q.A. GROM
34	Q.A. GROM
35	VIDEO GAMES U.K.
36	VIDEO GAMES U.K.
37	DEMONSTRATION (GERMAN)
38	DEMONSTRATION (GERMAN)
39	DEMONSTRATION (GERMAN)
40	DEMONSTRATION (GERMAN)
41	COMPUTER ART (GERMAN)
42	COMPUTER ART (GERMAN)
43	COMPUTER ART (GERMAN)
44	PHYSICAL FITNESS (GERMAN)
45	PHYSICAL FITNESS (GERMAN)
46	NUMBER MAGIC (GERMAN)
47	
48	
49	
50	TERMINAL EMULATOR
51	TERMINAL EMULATOR
52	
53	
54	
55	
56	
57	
58	
59	
60	PERSONAL RECORD KEEPING
61	PERSONAL RECORD KEEPING
62	PERSONAL RECORD KEEPING
63	PERSONAL RECORD KEEPING
64	STATISTICS
65	STATISTICS
66	STATISTICS
67	STATISTICS
68	STATISTICS
69	EARLY READING
70	EARLY READING
71	EARLY READING
72	EARLY READING
73	EARLY READING
74	SECURITIES ANALYSIS
75	SECURITIES ANALYSIS
76	SECURITIES ANALYSIS
77	SECURITIES ANALYSIS
89	DISK MANAGER
90	DISK MANAGER
91	WUMPUS
92	TIRK
93	TIRK
94	TIRK
95	TIRK
96	ECD WUMPUS

Grom Port I/O:

Cass. I/O ↑



Back 1-35 (1,3,5,etc)
Front 2-36 (2,4,6,etc) → I/O Port

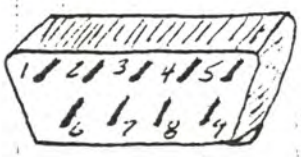
GROM I/O:

Back	Front
1 - Reset = -5 with grom in	2 - Ground
3 - D7	4 - $\overline{\text{CRU}}$ CLK
5 - D6	6 - $\overline{\text{CRU}}$ IN
7 - D5	8 - A15 CRU OUT
9 - D4	10 - A13
11 - D3	12 - A12
13 - D2	14 A11
15 - D1	16 - A10
17 - DØ	18 - A9
19 - +5V	20 - A8
21 - GROM Select	22 - A7
23 - A14	24 - A3
25 - DBIN	26 - A6
27 - GROM CLK	28 - A5
29 - -5V.	30 - A4
31 - GROM Ready	32 - $\overline{\text{WE}}$
33 - GROM Vss	34 - $\overline{\text{ROM G}}$
35 - Ground	36 - Ground

Schedule

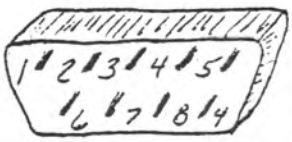
Cass./Joystick/Video-I/O Port

Cassette I/O:



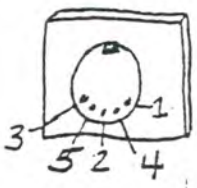
1- } CASSETTE 1
2- } MOTOR
3-(Ground) } Mag Out
5-
4-
6- } CASSETTE 2
7- } MOTOR
8- } Mag IN
9-(Ground) }

Joystick I/O:



1-
2- Joystick B
3- Key 0 (UP)
4- Key 4 (Push Button)
5- Key 3 (LEFT)
6-
7- Joystick A
8- Key 1 (DOWN)
9- Key 2 (RIGHT)

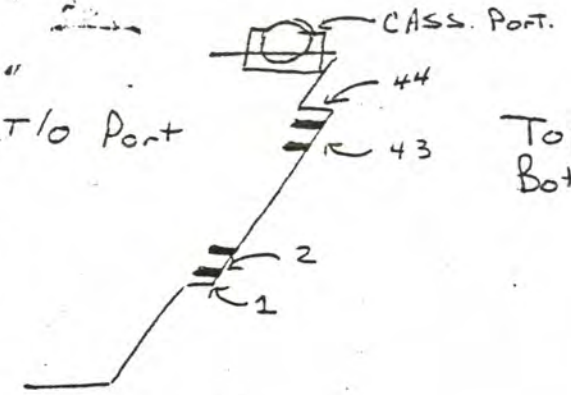
Video I/O:



1- +12V.
2- Ground
3- Sound Out
4- Comp. Video Out
5- Ground

Ron G.

I/O Port



I/O Port

Top = 2-44 (2, 4, 6, etc)
Bottom = 1-43 (1, 3, 5, etc)

I/O Port: Top

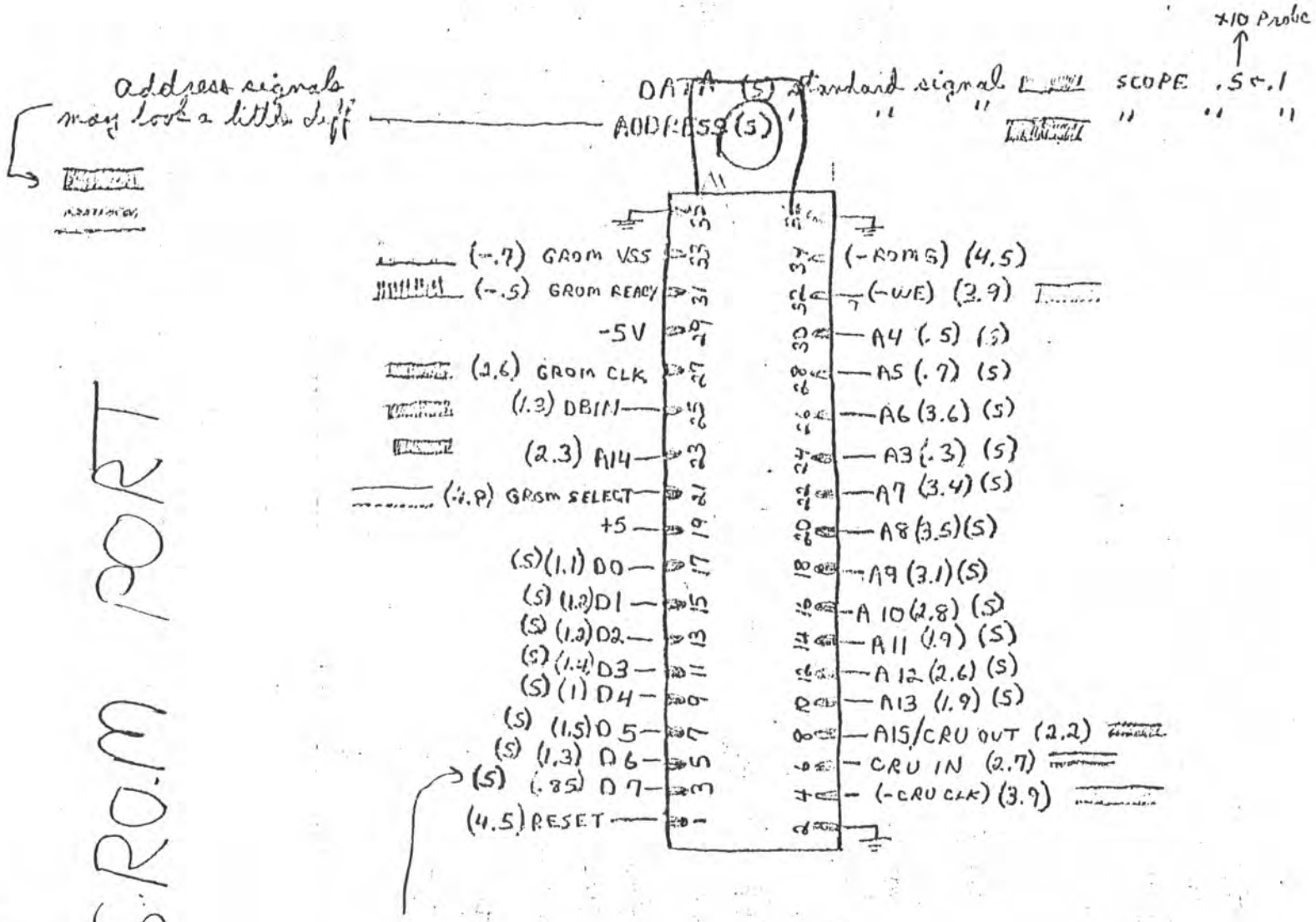
2 -	$\overline{SBE}$*
4 -	$\overline{Ext.\ Int.}$*
6 -	A10
8 -	A11
10 -	A3
12 -	Ready
14 -	A8
16 -	A14
18 -	A9
20 -	$\overline{A2}$
22 -	$\overline{CRU}$ CLK
24 -	$\overline{\phi 3}$
26 -	$\overline{WE}$
28 -	$\overline{MBE}$*
30 -	$\overline{A1}$
32 -	MEMEN*
34 -	D7
36 -	D6
38 -	D5
40 -	D1
42 -	D3
44 -	Sound In

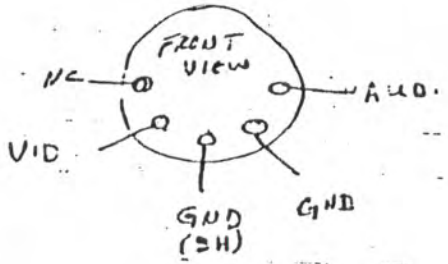
Bottom

1 -	+5 V.
3 -	Reset
5 -	A5
7 -	A4
9 -	DBIN*
11 -	$\overline{A12}$
13 -	LOAD
15 -	A13
17 -	A7
19 -	A15
21 -	Ground }
23 -	Ground }
25 -	Ground } 1 etch on I/O
27 -	Ground }
29 -	A6
31 -	Aϕ
33 -	CRU IN
35 -	D4
37 -	Dϕ
39 -	D2
41 -	Hold / IAQ*
43 -	-5V.

* SBE - Speech Block Enable
MBE - Memory Block Enable
Ext. Int - External Interrupt
Memen - Memory Enable
DBIN - Data Bus In
IAQ - Instruction Acquisition

Ron C.

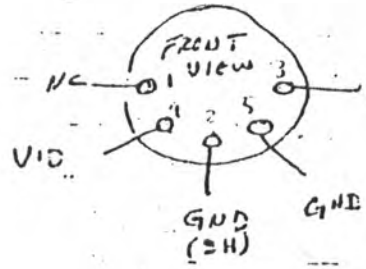

x10 Probe
address signals may look a little off
DATA (5) standard signal
ADDRESS (5)
" " "
SCOPE .5<.1
" " "
(-.7) GROM VSS
(-.5) GROM READY
-5V
(2.6) GROM CLK
(1.3) DBIN
(2.3) A14
(.4.9) GROM SELECT
+5
(5)(1.1) D0
(5) (1.2) D1
(5) (1.2) D2
(5) (1.4) D3
(5) (1) D4
(5) (1.5) D5
(5) (1.3) D6
(5) (.85) D7
(4.5) RESET
(-ROMS) (4.5)
(-WE) (3.9)
A4 (.5) (5)
A5 (.7) (5)
A6 (3.6) (5)
A3 (.3) (5)
A7 (3.4) (5)
A8 (3.5) (5)
A9 (3.1) (5)
A10 (2.8) (5)
A11 (1.9) (5)
A12 (2.6) (5)
A13 (1.9) (5)
A15/CRU OUT (2.2)
CRU IN (2.7)
(-CRU CLK) (3.9)
GROM PORT
5= signal



Box #1

CABLE #	# of cables
1	1
2	2
3	3
4	3
5	2
6	1

GND
GND
GND
GND



#1 — N.C.

2. — Video Ground

3 — Audio

4 — Video

5 — Audio Ground

GND
GND
GND
GND